LeCroy

2249A/SG/W

ME-8255

SERIES 2249A, SG, W

12-CHANNEL ADC

August 1982

WARRANTY

LeCROY RESEARCH SYSTEMS CORP. warrants each instrument it manufactures to be free from defects in material and workmanship under normal use and service for the period of 1-year from date of purchase. Custom monolithics and hybrids sold separately and all spare or replacement parts are warranted for 90-days. This warranty extends only to the original purchaser. This warranty shall not apply to fuses, disposable batteries or any product or parts which have been subject to misuse, neglect, accident or abnormal conditions of operations.

In the event of failure of a product covered by this warranty, LeCroy will repair and calibrate an instrument returned to the factory or an authorized service facility within 1 year of the original purchase; provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may, at its option, replace the product in lieu of repair. With regard to any instrument returned within one year of the original purchase, said repairs or replacement will be made without charge. If the failure has been caused by misuse, neglect, accident or abnormal conditions or operations, repairs will be billed at a nominal cost. In such case, an estimate will be submitted before work is started, if requested.

The foregoing warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness or adequacy for any particular purpose or use. LeCroy Research Systems Corp., shall not be liable for any special, incidental or consequential damages, whether in contract, tort or otherwise.

IF ANY FAILURE OCCURS, notify LeCroy Research Systems Corp., or the nearest service facility, giving full details of the difficulty, and include the Model number, serial number, and FAN (Final Assembly Number) or ECO (Engineering Change Order) number. On receipt of this information, service data or shipping instructions will be forwarded to you. On receipt of the shipping instructions, forward the instrument, transportation prepaid. A Return Authorization number will be given as part of shipping instructions. Marking this RA number on the outside of the package will insure that it goes directly to the proper department within LeCroy. Repairs will be made at the service facility and the instrument returned, transportation prepaid.

ALL SHIPMENTS OF LECROY INSTRUMENTS FOR REPAIR OR ADJUSTMENT should be made via Air Freight or "Best Way" prepaid. The instrument should be shipped in the original packing carton; or if it is not available, use any suitable container that is rigid and of adequate size. If a substitute container is used, the instrument should be wrapped in paper and surrounded with at least four inches of excelsior or similar shock-absorbing material.

IN EVENT OF DAMAGE IN SHIPMENT to original purchaser the instrument should be thoroughly inspected immediately upon original delivery to purchaser. All material in the container should be checked against the enclosed packing list. The manufacturer will not be responsible for shortages against the packing sheet unless notified immediately. If the instrument is damaged in any way, a claim should be filed with the carrier immediately. (To obtain a quotation to repair shipment damage, contact the LeCroy factory or the nearest service facility).

DOCUMENTATION DISCREPANCIES OR OMISSIONS. LeCroy Research Systems is committed to providing unique, reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, the Engineering Department at LeCroy is continually refining and improving the performance of products. While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and only rarely include minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

ANY APPLICATION OR USE QUESTIONS, which will enhance your use of this instrument will be happily answered by a member of our Engineering Services Department, telephone 914-425-2000 or your local distributor. You may address any correspondence to:

LeCroy Research Systems Corp., 700 S. Main Street,
Spring Valley, New York 10977, ATTN: Engineering Services Dept.

European Customers can contact:

LeCroy Research Systems Ltd.
Elms Court
Botley
Oxford OX9 2LP England

LeCroy Research Systems SA
81 Avenue Louis Casai
1216 Cointrin-Geneva
Switzerland

LeCroy Research Sys. S.a.r.l.
Avenue Du Parana
Z.A. De Courtaboeuf
F-91940 Les Ulis, France

LeCroy Research Systems GmbH
Treitschkestrasse 3
Postfach 10 37 67
69 Heidelberg
West Germany

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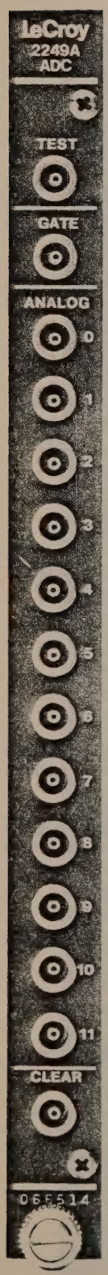
July, 1979

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York



CAMAC Model 2249A
12 Channel A-to-D Converter

FEATURES:

- **COMPACT PACKAGING**
  12 channels per single-width module means fewer crates, smaller systems, less gate fan-out.
- **WELL-CONTROLLED PEDESTAL**
  Advanced hybrid circuit front end eliminates peak shifts and/or constant calibration.
- **EXCELLENT INPUT IMPEDANCE MATCH**
  Minimizes possibility of digitizing input reflections.
- **10-BIT RESOLUTION**
  One part in 1024.
- **WIDEST DYNAMIC RANGE**
  4 times the range of 8-bit ADC's allows broader spectra, better accuracy, simplified setup, prevents small gain shifts from exceeding range of ADC.
- **HIGH SENSITIVITY**
  0.25 picocoulomb per count.
- **NO FEEDTHROUGH**
  Up to 1,000-fold overloads are rejected by fast gate, eliminating spurious data due to out-of-time chamber firings, noise, etc.
- **UNIFORM SENSITIVITY THROUGHOUT GATE INTERVAL**
  No modulation of measurement with position of signal within gate.
- **NO INTERCHANNEL CROSSTALK**
  regardless of input amplitude.
- **WELL-VENTILATED MODULE**
  Low component count, less than one-fifth of competing designs, permits free circulation of air for cooler, more reliable, and longer-lasting operation.
- **FAST CLEAR INPUT**
  enables fast rejection of unwanted data.
- **FULL TEST CAPABILITY**
  F(25) simultaneously injects charge into all ADC's proportional to DC level on front panel (or patch pins on Dataway).
- **FULL LAM FUNCTIONS.**
- **HIGH DIGITIZING SPEED**
  without sacrifice in differential linearity.
- **LAM AND Q SUPPRESSION**
  eliminates readout of empty modules.

The LRS Model 2249A 12-Channel Analog-to-Digital Converter embodies all the operational characteristics which have proved important for general-purpose use in high energy particle physics, including expanded resolution (0.1%), higher sensitivity, excellent stability, faster digitizing rate, LAM and Q suppression, provision for fast clear, calibrating test mode, and flexible LAM options.

These ADCs are specifically intended for use in demanding applications such as particle identification using dE/dx counters, recording x-ray, neutron, or recoil proton energies using lead glass or other total energy absorbtion counters, improving time resolution by correcting for slewing due to variances in counter output amplitudes, monitoring gas threshold Cerenkov counters, and debugging or monitoring proportional or drift chambers.

The Model 2249A contains twelve complete ADC's in a single-width CAMAC module. Each ADC offers a resolution of ten bits to provide 0.1% resolution over a wide 1024-channel dynamic range. The factor of 4 wider range allows operations with broad signal spectra such as are encountered in experiments anticipating fractionally charged particles or covering extensive energy ranges. It also greatly reduces the necessity for careful adjustment of signal strengths to match the limited range of an 8-bit, 256-channel instrument. The input sensitivity of the Model 2249A is 0.25 pC/count for a full-scale range of 256 pc. This is compatible with most available signal sources and no additional buffering or reshaping of any kind is required to digitize nanosecond pulses.

The excellent long-term stability, temperature characteristics, and isolation between ADC channels assure accurate and reliable performance under the demanding conditions encountered in actual experiments. Confirmation of operation and calibration is provided by the unique test feature which allows all twelve ADC's or an entire system to simultaneously digitize a charge proportional to a dc level provided to a front-panel Lemo connector or patched into P_1, P_2 or P_5 of the Dataway connector.

The Model 2249A offers excellent event rate capability through the incorporation of a fast clear and a fast digitizing rate. The fast clear input enables the ADC to begin digitizing on the command of a prompt gate and be reset, if necessary, before the end of conversion on the basis of delayed logic or chamber information. This feature eliminates the long input delay cables now required in these situations.

End of conversion of modules which contain data is flagged by generation of a CAMAC LAM. Readout of modules which do not contain information can be eliminated either by use of the LAM signals or through Q suppression.

August 1982

Innovators in Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, N.Y. 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

SPECIFICATIONS
Model 2249A
12 CHANNEL ADC

Analog Inputs: Twelve; Lemo-type connectors; charge-sensitive (current-integrating); direct-coupled, quiescently at approximately +4 mV; 50 Ω impedance; linear range normally −2 mV to −1 V; protected to ± 50 volts against 1 μsec transients.

Full-Scale Range: 256 pC ± 5%.

Full-Scale Uniformity: ± 5%.

Integral Non-linearity: ± .25% of reading ± 0.5 pC (12 pC to 256 pC) for >500 Ω source.

ADC Resolution: 10 bits actual, (0.1%).

Long-Term Stability: Better than 0.25% of reading ± 0.5 pC/week (at constant temperature).

Temperature Coefficient: Typical, 0; max., ± [.03% of reading (in pC) + .002t] pC/°C (where t = gate duration in nanoseconds, with 50Ω reverse termination).

ADC Isolation: A 5-volt, 20 ns overload pulse in any one ADC disturbs data in any other ADC by no more than 0.25 pC.

Gate Input: One gate common to all ADC's; LEMO-type connectors; 50 Ω impedance; −600 mV or greater enables; minimum duration, 10 ns; maximum recommended duration, 200 ns (actual limit approximately 2 microseconds with reduced accuracy; partial analog input must occur within 0.5 μsec after opening gate to preserve accuracy), effective opening and closing times: 2 ns; internal delay, 2 ns.

Fast Clear: One front-panel input common to all ADC's; LEMO-type connector; 50 Ω impedance; −600 mV or greater clears, minimum duration, 50 ns. (Caution: narrower pulses cause partial clearing.) Requires additional 2.0 μs settling time after clear.

Residual Pedestal: Typically 1 + 0.03t picocoulombs (where t = gate duration in nanoseconds) with 50 Ω reverse termination.

Test Function: With CAMAC I present, the positive DC level applied to front panel "Test" input (internal high impedance connection to +12 volts) or optional rear connector P1, P2, or P5 patch points will inject charge with a proportionality constant of −12.5 pC/volt into all inputs at F(25) • S2 time. (With CAMAC I not present, F(25) • S2 will generate the ≈80 ns gate only, providing a measure of residual pedestal only.)

Digitizing Time: 60 μs. By factory option, 8-bit operation at 12.5 μs digitizing time may be provided.

Readout Time: Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.

Readout Control: Ready for readout when LAM signal appears. Refer to ESONE Committee Report EUR4100e and EUR4600e for additional timing details, voltages, logic levels, impedances, and other standards.

Data: The proper CAMAC function and address command normally gates the 10 binary bits plus overflow bit of the selected channel onto the R1 to R11 (2^0 to 2^{10}) Dataway bus lines.

CAMAC Commands:

Z or C: ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. Z also disables LAM.
I: Gate input is inhibited during CAMAC "Inhibit" command. (Test Function is enabled.)
Q: A Q=1 response is generated in recognition of an F(0) or F(2) Read function or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q=0) under any other condition. The Q response for empty modules can be suppressed. (See Q and LAM suppression.)
X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated.
L: A Look-At-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by Test LAM. Standard option causes LAM to be suppressed for empty modules.

CAMAC Function Codes:

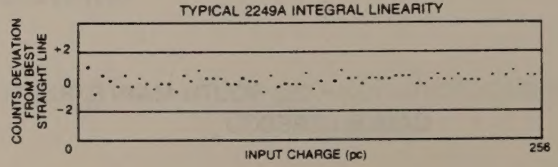
F(0): Read registers; requires N and A, A(0) through A(11) are used for channel addresses.
F(2): Read registers and Clear module and LAM; requires N and A; (Clears on A(11) only.)
F(8): Test Look-At-Me; requires N and any A from A(0) to A(11) independent of Disable Look-At-Me. Q response is generated if LAM is set.
F(9): Clear module and LAM; requires N, S2, and any A from A(0) to A(11).
F(10): Clear Look-At-Me; requires N, S2, and any A from A(0) to A(11).
F(24): Disable Look-At-Me; requires N, S2, and any A from A(0) to A(11).
F(25): Test module; requires N, S2, and any A from A(0) to A(11).
F(26): Enable Look-At-Me; requires N, S2, and any A from A(0) to A(11). Remains enabled until Z or F(24) applied.
Caution: The state of the LAM mask will be arbitrary after power turn-on.

Q and LAM Suppression: Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered useful. A module in which all channels contain less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.

Packaging: In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e). RF shielded CAMAC #1 module.

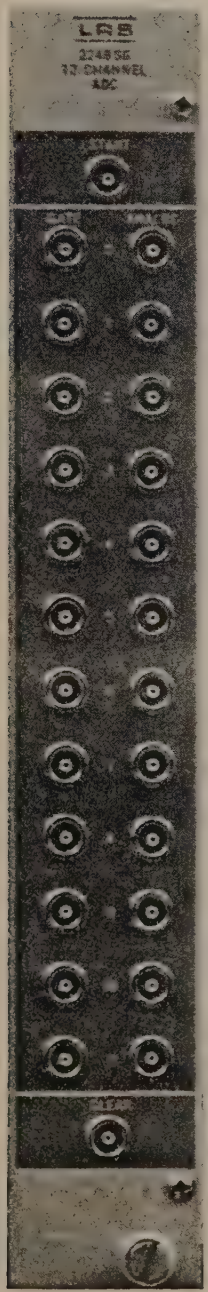
Current Requirements: +24 V at 35 mA; −24 V at 15 mA; +6 V at 850 mA; −6 V at 200 mA.

TYPICAL 2249A INTEGRAL LINEARITY



SPECIFICATIONS SUBJECT TO CHANGE.

LeCroy
RESEARCH SYSTEMS



CAMAC Model 2249SG
12-Channel A-to-D Converter With Separate Gates

The LeCroy Model 2249SG 12-Channel Analog-to-Digital Converter is a separately gated version of the world's most widely used integrating ADC, the Lecroy Model 2249A. It embodies all the operational characteristics which have proved important for general-purpose use in high energy particle physics, including high resolution, high sensitivity, excellent stability, fast digitizing rate, LAM and Q suppression, provision for fast clear, calibrating test mode, and flexible LAM options.

The Model 2249SG contains twelve complete ADC's in a double-width CAMAC module. Each ADC offers a 10-bit conversion to provide a wide 1024-channel dynamic range. The input sensitivity of the Model 2249SG is 0.25 pC/count for a full-scale range of 256 pC. This is compatible with most available signal sources and no additional buffering or reshaping of any kind is required to digitize nanosecond pulses.

The excellent long-term stability, temperature characteristics, and isolation between ADC channels assure accurate and reliable performance under the demanding conditions encountered in actual experiments. Confirmation of operation and calibration is provided by a unique optional test feature which allows all twelve ADC's or an entire system to simultaneously digitize a charge proportional to a dc level provided to a front-panel Lemo connector or patched into P_1, P_2, or P_5 of the Dataway connector.

The Model 2249SG offers excellent event rate capability through the incorporation of a fast clear and a fast digitizing rate. The fast clear input enables each ADC to begin digitizing on the command of a prompt gate and be reset, if necessary, before the end of conversion on the basis of delayed logic or chamber information. This feature eliminates the long input delay cables now required in these situations.

End of conversion of modules which contain data is flagged by generation of a CAMAC LAM. Readout of modules which do not contain information can be eliminated either by use of the LAM signals or through Q suppression.

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Innovators in Instrumentation

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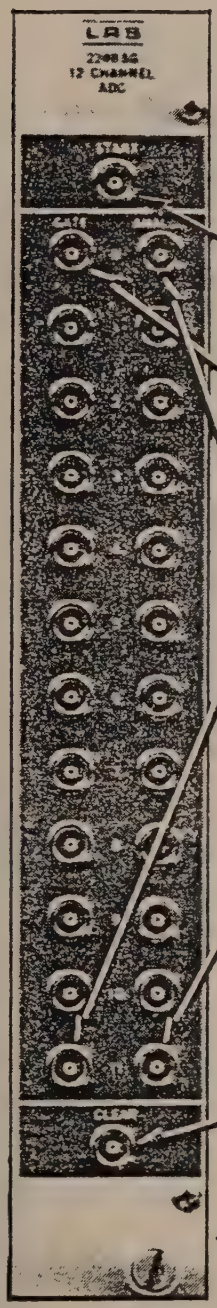
TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

SPECIFICATIONS
MODEL 2249SG
12-CHANNEL ADC WITH SEPARATE GATES

Analog Inputs:	Twelve, Lemo-type connectors; charge-sensitive (current-integrating); direct-coupled, quiescently at approximately +4 mV; 50 Ω impedance; linear range normally −2 mV to −1 V; protected to ± 50 volts against 1 μsec transients.
Full-Scale Range:	256 pC.
Full-Scale Uniformity:	± 5%.
Integral Non-linearity:	±0.25% of reading ±0.5 pC.
ADC Resolution:	10 bits (0.1%) somewhat degraded to approx. 0.2% by clock unsynchronized with any specific linear gate input.
Long-Term Stability:	Better than 0.25% of reading ±0.5 pC/week (at constant temperature).
Temperature Coefficient:	Typical, 0; max., ±(.03% of reading (in pC) +0.002 t) pC/°C (where t=gate duration in nanoseconds, with 50 Ω reverse termination).
ADC Isolation:	A 5-volt, 20 nsec overload pulse in any one ADC disturbs data in any other ADC by no more than 0.25 pC.
Gate Inputs:	Twelve, one per ADC; Lemo-type connectors; 50 Ω impedance; −1.4 V or greater enables; minimum duration, 10 nsec; maximum recommended duration, 200 nsec (actual limit approximately 2 microseconds with reduced accuracy; partial analog input must occur within 0.5 μsec after opening each gate to preserve accuracy), effective opening and closing times; 2 nsec; internal delay, 2 nsec. All gates should occur within 2 μsec of the "start" pulse (other arrangements require internal resistor change). CAUTION: Subsequent gate signals are NOT INHIBITED after receipt of the first one, so care must be taken to externally prevent the application of more than one gate to each channel until a clear is applied.
Start Input:	A NIM level (> −600 mV) signal of a duration exceeding 10 nsec must be applied to start the internal oscillator. It should be applied simultaneous to the earliest gate pulse or should follow it by no more than 100 nsec.
Fast Clear:	One front-panel input common to all ADC's; Lemo-type connector 50 Ω impedance; −600 mV or greater clears, minimum duration, 50 nsec. (Caution: narrower pulses cause partial clearing.) Requires additional 1.5 μsec settling time after clear.
Test Function:	The standard 2249SG does not respond to F(25) and has no test feature. However, on-line test capability is optional at the expense of the CAMAC "Inhibit". With Q7 (the "inhibit" transistor) removed, the leading edge of a pulse applied to the "start" input will cause a fixed charge to be injected onto the 2249SG analog inputs. Coincident with the "start," the 12 gate pulses must be applied of duration approximately 80 nsec. Proportionality constant is −12.5 pC/volt of dc signal applied to P1, P2 or P5 patch points, for an 80 nsec gate. In this test mode, the gates must precede the "start" by 10 nsec.
Digitizing Time:	Approximately 60 μsec.
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.
Readout Control:	Ready for readout when LAM signal appears. Refer to ESONE Committee Report EUR4100e and EUR4600e or IEEE #583 for additional timing details, voltages, logic levels, impedances, and other standards.
Data:	The proper CAMAC function and address command normally gates the 10 binary bits plus overflow bit of the selected channel onto the R1 to R11 (2^0 to 2^{10}) Dataway bus lines.
CAMAC Commands:	Z or C: ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. I: Gate input is inhibited during CAMAC "Inhibit" command. (Nonfunctional if unit is modified to provide "Test" feature.) Q: A Q=1 response is generated in recognition of an F(0) or F(2) Read function or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q=0) under any other condition. The Q response for empty modules can be suppressed. (See Q and LAM suppression.) X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: A Look-At-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by Test LAM. Standard option causes LAM to be suppressed for empty modules.
CAMAC Function Codes:	F(0): Read registers; requires N and A, A(0) through A(11) are used for channel addresses. F(2): Read registers and Clear module and LAM; requires N and A; (Clears on A(11) only.) F(8): Test Look-At-Me; requires N and any A from A(0) to A(11) independent of Disable Look-At-Me. Q response is generated if LAM is set. F(9): Clear module and LAM; requires N, S2, and any A from A(0) to A(11). F(10): Clear Look-At-Me; requires N, S2, and A from A(0) to A(11) F(24): Disable Look-At-Me; requires N,S2, and any A from A(0) to A(11). F(26): Enable Look-At-Me; requires N, S2, and any A from A(0) to A(11). Remains enabled until Z or F(24) applied. Caution: The state of the LAM mask will be arbitrary after power turn-on.
Q and LAM Suppression:	Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered useful. A module in which all channels contain less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e or IEEE Report #583). RF-shielded CAMAC #2 module.
Current Requirements:	+24 V at 35 mA; −24 V at 15 mA; + 6 V at 850 mA; −6 V at 200 mA.

CAMAC Model 2249SG

12-Channel A-to-D Converter With Separate Gates



START Inputs: Requires >-600 mV (into 50 Ω) fast NIM-level signal of duration >10 nsec. (Should be applied 0 - 100 nsec after the earliest gate pulse).

GATE Inputs: Require >-1.4 volts (into 50 Ω) to enable; all gates must start within 2 μsec of "start" pulse.

12 ANALOG Inputs: Duration 0 - 200 nsec; amplitude linear range, 0 to -1 volt; impedance = 50 Ω.

Fast CLEAR: Fast NIM level, >-600 mV into 50 Ω; minimum duration 50 nsec (1.5 μsec settling time required after clear).

CAMAC #2 width module.

April, 1977

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

CAMAC Model 2249W
12-Channel A-to-D Converter

The LeCroy Model 2249W is a twelve-channel, eleven-bit integrating-type analog-to-digital converter. It features excellent linearity and unprecedented stability, thus allowing operation at wide gates of up to 10 μsec. Thus, the 2249W is compatible with CsI and NaI crystal detectors. Its minimum gate of 30 nsec makes its use with organic scintillators and Čerenkov detectors possible in all but the highest rate conditions.

The 2249W has been optimized for dynamic range and linearity. By AC-coupling the input, 11 bit (1980 counts) operation has been achieved with $\pm$ 1 count integral linearity. This excellent linearity is maintained from the smallest signal size to signals as large as -2 V.

The test feature allows all twelve ADC's to simultaneously digitize a charge proportional to a DC-level provided to a front-panel connector or patched into the CAMAC Dataway connector. In addition, the pedestals alone can be checked on-line by the same test feature by removing the CAMAC inhibit (I) during the test.

The Model 2249W offers an excellent event rate capability through the incorporation of a 2 μsec fast clear, which permits the ADC's to begin digitizing and then be cleared upon receipt of later trigger information rather than delaying the analog signals with long cables while the trigger decision is being made. In addition, rapid readout is made possible by a convenient Q and LAM suppress feature, side-panel adjustable between 0 and 100 counts. This feature permits an empty 2249W to be overlooked in a CAMAC readout cycle.

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Innovators in Instrumentation

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TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

SPECIFICATIONS
CAMAC Model 2249W
12-CHANNEL A-TO-D CONVERTER

Analog Inputs:	Twelve: LEMO-type connectors; charge-sensitive (current-integrating); AC-coupled (30 μsec time constant, field changeable); 50 Ω impedance; linear range normally 0 to −2.0 V; protected to ± 50 volts against 1 μsec transients.
Gain:	−0.25 pC/count ± 5%.
Full-Scale Range:	Approximately −500 pC (maximum count ≅ 1980).
Integral Non-Linearity:	± 0.05%.
ADC Resolution:	0.05% (1980 total counts).
Long-Term Stability:	Better than 0.25% of reading ± 0.5 pC/week (at constant temperature).
ADC Isolation:	A 5 volt, 20 nsec overload pulse in any one ADC disturbs data in any other ADC by no more than 0.5 pC (2 counts).
Gate Input:	One gate common to all ADC's; LEMO-type connectors; 50 Ω impedance; −600 mV or greater enables; minimum duration, 30 nsec; maximum recommended duration up to 10 μsec; partial analog input must occur within 0.5 μsec after opening gate to preserve accuracy; effective opening and closing times: 5 nsec; internal delay, 7 nsec.
Fast Clear:	One front-panel input common to all ADC's; LEMO-type connector; 50 Ω impedance; −600 mV or greater clears, minimum duration, 50 nsec. Requires additional 2.0 μsec settling time to settle to within 2 counts after clear.
Pedestal:	Adjustable over approximately 100 counts via side-panel accessed trimmer capacitor. Actual value depends upon gate duration.
Test Function:	With CAMAC I present, the positive DC level applied to front-panel "Test" input (internal high impedance connection to +12 volts) or optional rear connector P1, P2,, or P5 patch points will inject charge with a proportionality constant of −20 pC/volt into all inputs at F(25)•S2 time. (With CAMAC I not present, F(25)•S2 will generate the gate only, providing a measure of the pedestal.)
Digitizing Time:	106 μsec.
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.
Readout Control:	Ready for readout whem LAM signal appears. Refer to ESONE Committee Report EUR4100e and EUR4600e for additional timing details, voltages, logic levels, impedances, and other standards.
Data:	The proper CAMAC function and address command normally gates the 11 binary bits of the selected channel onto the R1 to R11 (2^0 to 2^{10}) Dataway bus lines.
CAMAC Commands:	Z or C: ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. Z also disables LAM. I: Gate input is inhibited during CAMAC "Inhibit" command. (Test function is enabled.) Q: A Q=1 response is generated in recognition of an F(0) or F(2) Read function or an F(8) function if LAM is set for a valid "N" and "A," but there will be no response (Q=0) under any other condition. The Q response for empty modules can be suppressed (see Q and LAM suppression). X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: A Look-At-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by test LAM. Standard option causes LAM to be suppressed for empty modules.
CAMAC Function Codes:	F(0): Read registers; requires N and A; A(0) through A(11) are used for channel address. F(2): Read registers and Clear module and LAM; requires N and A; (clears on A(11) only). F(8): Test Look-At-Me; requires N and any A from A(0) to A(11) independent of Disable Look-At-Me. Q response is generated if LAM is set. F(9): Clear module and LAM; requires N, S2, and any A from A(0) to A(11). F(10): Clear Look-At-Me; requires N, S2, and any A from A(0) to A(11). F(24): Disable Look-At-Me; requires N, S2, and any A from A(0) to A(11). F(25): Test module; requires N, S2 and any A from A(0) to A(11). F(26): Enable Look-At-Me; requires N, S2, and any A from A(0) to A(11). Remains enabled until Z or F(24) applied. Caution: the state of the LAM mask will be arbitrary after power turn-on.
Q and LAM Suppression:	Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered useful. A module in which all channels contain less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accept response is still generated. The LAM suppress portion can be disabled with a solder jumper option.
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e). RF shielded CAMAC # 1 module.
Current Requirements:	+24 V at 143 mA; −24V at 75 mA; +6 V at 725 mA; −6 V at 155 mA.

4. OPERATIONAL DESCRIPTION

4a. General

The LeCroy Model 2249 Series 12-Channel ADC contains 12 complete analog-to-digital converters in a single-width CAMAC module. The 2249A and SG offer 10 bits, and the W version offers 11 bits. The analog-to-digital conversion is accomplished by the Wilkinson-rundown method, which ultimately yields a digital output (in TTL negative logic binary format) which is proportional to the integral of the i·dt of the input pulse. By the Wilkinson technique, the input charge is delivered to an integrating capacitor from a linear gate, and then discharged at a constant rate. During the time this rundown is taking place, pulses from an oscillator are gated into a scaler resulting in the final count proportional to the charge originally stored in the capacitor.

4b. Analog Inputs

The 12 analog inputs of the 2249 Series are of 50 Ω impedance and accept negative-going pulses or levels only during an externally applied gating interval. To assure performance within the linear range of the 2249A and SG, input signals should not exceed -1 volt or 2 volts for the W version. The actual amount of input charge that yields a full scale digital output (1024 counts) is 256 picocoulombs (or 12.8 volt-nsec) for the 2249A and SG (512 pC, 25.6 volt-nsec, for the W version). The full scales of the 12 channels of each 2249 are set up to match within 5% of each other. Quiescent DC level of the anlog inputs of the 2249A and SG are set at approximately +4 mV to assure that it does not go negative should any drift occur. The 2249W is AC coupled and does not require this critical biasing.

4c. Gate

The built-in linear gate is common to all 12 analog inputs of the A and W, necessitating that analog-to-digital conversion for all channels is done in parallel. The 50 Ω impedance gate accepts pulses $\geq$-600 mV in amplitude. The duration may be between 10 nsec and 200 nsec (see next paragraph). Because of the finite risetime and falltime of the internal gate pulse, the effective gating interval is not adequately defined to allow input gate pulses shorter than 10 nsec. The actual gate opening

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and closing times are approximately 2 nsec, and the gate should precede the analog inputs by at least 4 nsec (A & SG versions) or 7 nsec (W version). Except when photomultiplier noise is a prime consideration, it is good practice to apply a gate pulse which is wider than the expected duration of the longest analog input. IMPORTANT NOTE! The duration of the effective gate will exceed that of the gate pulse by 4 nsec for the A and SG versions and 5 nsec for the W version.

For the 2249A and SG, gate widths exceeding 200 nsec create excessive residual pedestal (1 + 0.03t/pC, where t = gate duration in nanoseconds) and reduce the overall accuracy of the ADC by magnifying the effects of the instability manifest in the temperature coefficient, which is directly dependent upon the gate width, (i.e., maximum of ± (.03% of reading (in pC) + .002 t)pC/^{o}C). In addition, longer gates will imply an increased susceptability to any DC offset of the analog input. The actual limit of the gate duration is 2 μsec provided the resultant decrease in accuracy can be tolerated. Actually, with a gate duration of >200 nsec, it is recommended that the inputs be AC-coupled if possible.

The excellent stability and linearity of the Model 2249W allows it to be used with gate widths up to 10 μsec. In order to maintain this linearity with wide gates, however, it is necessary for the input pulse to occur within 500 nsec of the gate opening. During this 500 nsec period, a fixed amount of charge is automatically injected onto the integrarating capacitor to assure linear operation even for very small input charges which would otherwise deviate from the linearity maintained by the circuit for larger input charges. This injection lasts approximately 500 nsec, but the appearance of charge from the analog input will cause it to be extended. Without input charge appearing, the q inject will cease after 500 nsec (i.e., charge added will settle out), and subsequent input charge would be subject to a conversion graph which goes non-linear at the bottom (i.e., for small input charges).

Similarly, if it is necessary to use wide gates (>200 nsec) and the 2249W is not available, the 2249A must be used with reduced accuracy, then the analog input should occur within 500 nsec after the gate opening. During this 500 nsec period, a fixed amount of charge is automatically injected into the integrating capacitor to assure linear operation in a region representing very small input charge which would otherwise deviate from the linearity maintained by the circuit for larger input charges. This charge

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injection lasts only 500 nsec, but the appearance of charge from the analog input will cause it to be extended. Without input charge appearing, the q inject will cease after 500 nsec (i.e., charge added will settle out), and subsequent input charge would be subject to a conversion graph which goes nonlinear at the bottom (i.e., for small input charges).

The 2249 Series gate is inhibited from shortly (≈100 nsec) after the trailing edge of the gate until any CAMAC clear (C, Z, F(9) or F(2)·A(11)) or a front panel clear is applied. This effectively locks out spurious analog signals and noise from the ADC while the desired signal is being processed. The ADC's internal oscillator is synchronized with the leading edge of the gate pulse (although it occurs somewhat later), eliminating inaccuracies caused by the utilization of free-running oscillators in previous designs.

The 2249SG gate inputs require -1.4 V to be enabled. Deviations from this amplitude will result in pedestal variations as the charge injection is controlled by the gate pulse. The gate inputs are terminated in 50 Ω allowing one half of the 32 mA current source output of a NIM module (such as the LeCroy Model 821) to be employed. The second half of the bridged pair should not be terminated in 50 Ω.

4d. Start Input (2249SG Only)

Because the gate inputs of the 2249SG are considered asynchronous, a separate signal is required to start the internal oscillator. This pulse should be a NIM level applied either simultaneously with the earliest gate pulse or should follow it by ≤100 nsec. The pedestal of a given channel will decrease by 1 count per 50 nsec start delay,with respect to the Gate time.

4e. Fast Clear

A front panel fast clear input accepting fast NIM-level signals (≥600 mV into 50 Ω of minimum duration, ≥50 nsec) forces all 12 channels to cease their conversions, be cleared and ready to accept another gate pulse after 1.2 to 1.5 μsec. In worst-case conditions, the 2249A and SG will clear to within 1 count after 1.2 μsec. An internal monostable makes the 1.2 μsec period mandatory, although this can be changed by special request at a sacrifice in the extent of the clearing. The fast clear feature allows ADC conversion to begin by a fast trigger and completed only if the event satisfies a complete trigger requirement.

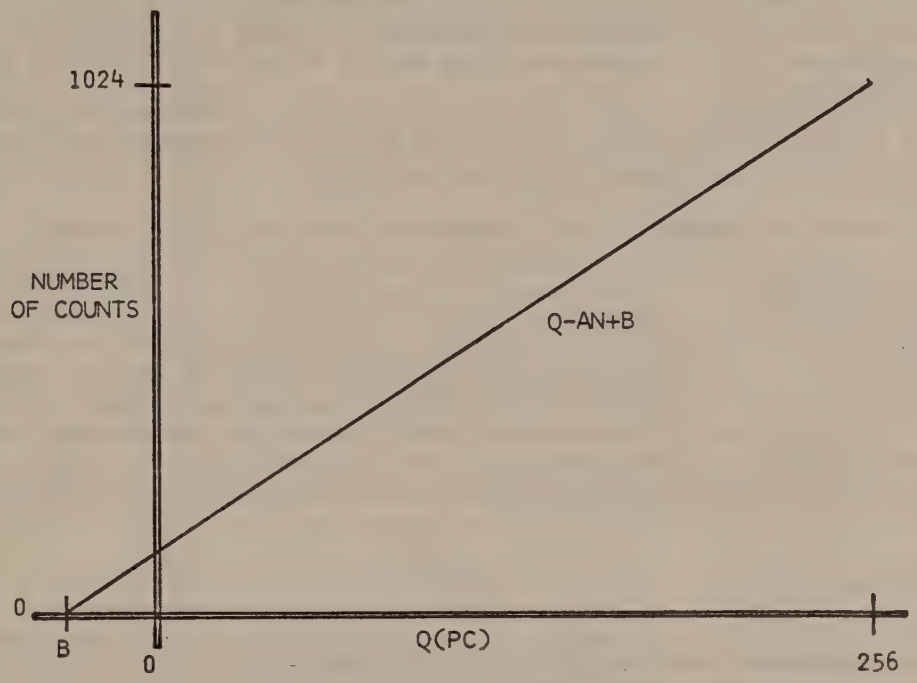
4f. Test Feature

A built-in test feature checks all channels simultaneously with an F(25) command. If the CAMAC Inhibit (I) is present and a positive DC level is applied either to a front panel "Test" input (with internal high Z (≥10KΩ) connection to a +12 volts) or optionally to rear connector patch points P1, P2, or P5, then F(25)·S2 will inject charge with a proportionality constant of -12.5 pC/volt into all inputs (23.5 pC for the W version). The internal gate generated by F(25)·S2 is approximately 80 nsec. If the user desires a measure of residual pedestal only, the CAMAC "I" should be removed; F(25)·S2 will then generate the 80 nsec gate only with no charge being injected into the analog inputs. This test feature permits the pedestal itself to be periodically checked for drifts. If two measurements are made, one with charge input and one without (i.e., with and without "I"), the total conversion characteristics could be checked. In this case, the "no charge" result gives the intercept and the "with charge" counts minus the "without charge" counts divided by the charge applied, gives the slope of the conversion plot. (See Graph on next page.)

The test feature may be connected to the rear of the 2249 as mentioned previously. The rear of the 2249 printed circuit board contains 3 drilled holes labeled P1, P2 and P5. Soldering a feedthrough through any one of these holes electrically connects the front panel "Test" input to the CAMAC connector pins P1, P2, or P5. In this way, many units can be grouped for simultaneous calibration.

It should be noted that the standard 2249SG does not respond to F(25) and has not "Test" feature. It is possible, however, to do on-line testing of the 2249SG if necessary. The price of this feature is the elimination of the inhibit feature. With the standard 2249A, the CAMAC "Inhibit" enabled the test circuit while disabling the gate circuit. Since the 2249SG has no internally generated "Test" function, the "Start" circuit must be used. To permanently enable this "Start" circuit to permit a test function to be performed, Q7, or the inhibit transistor, must be removed.

With Q7 removed, the leading edge of a pulse applied to the "Start" input will cause a fixed charge to be injected into the 2249SG analog inputs. Coincident with the "Start", the 12 gate pulses must be applied, which should have a duration between 80 nsec and 100 nsec. An exact 80 nsec gate will yield a proportionality constant of -12.5 pC/volt of DC signal



B IS AMOUNT OF PEDESTAL

Q IS CHARGE APPLIED TO ADC
ANALOG INPUTS

N IS TOTAL NUMBER OF COUNTS

A IS CONVERSION SLOPE
I.E. A-(Q+B)/N

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applied to whichever rear patch point (P1, P2, or P5) you choose to use for the test input. For shorter gate widths, a smaller net amount of charge is injected into each input, i.e., on the order of 90% ±1% for a 40 nsec gate.

If a test function is to be used, care must be taken to be sure the "gates" precede the "Start" by 10 nsec.

CAUTION: Since the "test" is not a designated feature of the 2249SG, its utilization is not factory tested.

4g. Linearity

The integral linearity of the 2249 Series is typically < ±2 counts (see specifications). This is defined by LeCroy as the maximum deviation from the best straight line fit to measured points. Every ADC is computer tested before being shipped to make certain it meets linearity and functional operation specifications. Each channel is tested for linearity at 50 points across its range by a 16 bit digital to charge converter.

4h. Pedestal

The residual pedestal is the number of counts obtained when a gate pulse is applied with a no analog input (i.e., input merely terminated in 50 Ω). Pedestal is a result of several factors, the largest of which is the charge injection (also contributing to the A and SG versions is a factory-set positive DC offset) the purpose of which is to assure proper operation of the front end in case the quiescent DC level of the input should drift. It is this DC offset contribution which largely comprises the gate-dependent portion of the residual pedestal specification. The fixed amount of pedestal indicated on the spec results largely from the q injection.

Due to DC coupling of the A and SG inputs, the gate-dependent portion of the pedestal has a temperature coefficient associated with it. This effect is magnified by a factor of 2 if the input is DC shorted to ground as it would be when driven from a pulse transformer, for example, used to cater photomultiplier dynode signals to the negative input requirements of the 2249A. For short gate widths, the resultatn potential temperature drift is small. However, it is nevertheless recommended that AC-coupling be used wherever rate conditions can permit it. This will nearly eliminate

all but the fixed pedestal and its associated temperature coefficient.

The pedestal of the 2249A is factory adjusted to 8 counts for a gate duration of 50 nsec and to 50 counts for the SG version. The adjustment is made with a 50 Ω termination of each analog input. The pedestal of each channel of the 2249A is separately screwdriver adjustable through the side panel. Each adjustment screw is accessed through a hole adjacent to the input for the channel. (NOTE: When making adjustments, use a non-conducting screwdriver.)

The pedestal of the 2249W is factory adjusted to 16 counts for a gate duration of 400 nsec. The adjustment is made with a 50 Ω termination of each analog input. The pedestal of each channel of the Model 2249W is also screwdriver adjustable through the side panel. Each adjustment screw is accessed through a hole in the input for the channel.

NOTE: When making adjustments, use a non-conducting screwdriver.

The pedestal dependence on gate width (t) is approximated as follows for the Model 2249W:

$$\text{PED Counts} = A_0(1-e^{-A_1 t/to}) + A_2 t + A_3$$

The first term is the exponential decay of the charge injected by the leading edge of the gate to bring the QTC into linear operation. A_0 and A_1 are proportional to the capacitance selected on the pedestal adjust trim cap in each channel. This trim accounts for only a few counts at 250 nsec and is less than one count from A_0 by 500 nsec. The effect of this trim can be reduced by reducing the setting of the pedestal adjust.

The second term, $A_2 t$, shows the linear relationship of pedestal to gate width above gate widths of 250 nsec. The factor A_2 is approximately 25 counts per microsecond. This small number reduces the need for stable gate widths.

The last term, A_3, is negative and represents the amount of charge that needs to be injected to put the QTC into linear operation and to compensate for gate width stretching (5 nsec) and the charge drained off before the clock starts. All of these terms vary slightly with different channels.

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4i. Conversion Time

Since the full scales of the 12 channels of each 2249 may differ from each other by up to ±5%, the time for each channel to achieve a full scale conversion may also differ from that of the other channels. Total conversion time is roughly 50 µsec for the A and SG versions and 100 µsec for the W version. Manufacturing variances in clock frequency, ramp currents, and the necessity to allow for overflow as well as a wait interval incorporated in the design, require that a 20% margin in conversion time be allowed for. As a result, the 2249A clock is internally held on for a maximum time of 60 µsec, the SG for 55 µsec, and the W for 100 µsec (for any size conversion). Due to the fast clear feature of the 2249, however, this conversion time need be awaited only for valid events.

A factory option for the 2249A allows 8-bit operation with 66 pC full scale (0.25 pC/count) and a conversion time of 16.5 ±5% µsec.

IMPORTANT: Care should be taken to ensure that all gates come within 2 µsec of the "Start" pulse. If this will not be true, the duration of active clock may be increased by changing the 20K Ω resistor on IC "TD" (9602) to a larger value. Then the maximum allowable time between any two gates should be the new value of the monostable delay minus approximately 53.5 µsec.

4j. Q and LAM Suppression

The 2249 Series was designed to permit one to eliminate the readout of empty modules if maximum readout rate is desired. An adjustable potentiometer (accessed from side of module) permits the user to define an "empty" module by setting a count level from 0 to 100 that must be accessed before data is considered useful. A module in which all channels contain less than the set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated.

Some branch drivers (interfaces between computer and CAMAC crate) require a Q response or a LAM from any module that occupies a station (N) in the CAMAC crate. For these situations, the L suppress feature may be defeated by removing the jumper XZ and replacing it with jumper YZ. (See Schematic

sheet 3 or the circuit board section on next page.) In this situation a LAM condition is obtained after any Read command. The Q-response suppress can be defeated by removing jumper VW and replacing it with jumper UW. To defeat both Q and L Suppress, it is only necessary to set the count level to 0. (NOTE: 2249's and older 2249A's do not have all the jumper options available on the P.C. board. These units will require the bus be cut and a jumper added on the solder side of the board.)

4k. Data and Readout

The output data of the 2249 Series is standard CAMAC compatible (TTL negative logic) in binary format, plus overflow. The digitized information plus overflow bit are gated onto the Dataway bus lines by F(0)·N·A, where F(0) signifies the read function, N signifies the 2249 to be read, and A (from A(0) to A(11)) signifies which ADC channel in the 2249 is to be read out. Generally the unit is ready for readout when LAM appears. The function F(2) (Read and Clear) may also be used to read information from chosen ADC channels. However, this readout is destructive only when A(11) is addressed, the F(2)·N·A(11) clearing all channels at one time. The F2 command on addresses A(0) through A(10) will cause the ADC contents to be read with no clear and the input gate will remain disabled.

41. LAM

A LAM (Look-At-Me) signal is generated from end of conversion until a module Clear or Clear LAM (Z, C, F(2), F(9) or F(10)). LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable F(26) or Disable F(24) function command, and can be tested by Test LAM F(8). LAM may be suppressed for empty modules as indicated in "Q and LAM Suppression" section above.

The test function F(8) allows the LAM to be tested. In response to application of F(8)·N·A (where A is any A from A(0) to A(11)) independent of Disable LAM, a Q response will be generated if LAM is set. Although the LAM is disabled while the 2249 in question is being addressed (i.e., for the duration of N), once latched it will produce a Q response when an F(8)·N·A is applied.

IMPORTANT! When current is applied to the 2249 (such as would occur when plugging a module in and turning the crate power supplies on),

JUMPER LOCATION SIMILAR ON ALL 2249 SERIES UNITS

the states of the LAM latch and LAM enable are arbitrary. The unit must always be initialized with an F(24) (Disable LAM) or an F(26) (Enable LAM), and an F(10) (Clear LAM).

4m. Packaging and Current Requirements

The 2249 is packaged in a standard #1 width CAMAC module (conforming to ESONE Committee Report EUR4100). The A and SG versions dissipate a total of 7.5 watts and the W, 10.6 watts.

CAUTION! Because of the adjacency of the various voltage bus connector contacts, plugging in any CAMAC unit may cause mementary misalignment of the unit and short the power pins to each other. This can cause severe damage to the module inserted, especially since the 24 volt pins are adjacent to the 6 volt pins. THUS, THE CRATE POWER SHOULD BE OFF WHEN A MODULE IS INSERTED OR REMOVED.

4n. Inhibit Circuit

The standard 2249A and W have an automatic inhibit that prevents subsequent gate pulses from allowing more charge to enter the QTC after a first gate pulse is applied. This "self inhibiting" feature is not offered on the 2249SG. Therefore, extreme caution must be taken to permit only one gate pulse per channel per event.

The Inhibit line of the 2249SG only affects the "Start" input, not the individual gates. Thus, gate pulses received during an inhibit period will cause charging of the integrating capacitor of the QT100C but no counts will be observed at the digital output.

Caution! Be sure that your gate pulse source is externally inhibited whenever a CAMAC inhibit is applied. This function is easily performed if LeCroy Model 821 Quad Discriminator with Veto is chosen to drive the ADC gates.

5. FUNCTIONAL DESCRIPTION

5a. General

The Model 2249 consists of 12 independent identical ADC's and associated circuitry. Referring to the 2249 Block Diagram following, the 2249 circuitry is divided into 6 basic parts:

- Twelve QTC (charge-to-time converter) channels
- A gate, test, and pedestal circuit for distributing the gate signal to the eight separate linear gates of the QTC's
- Twelve clock synchronizers and scalers
- A controller oscillator
- A Q response and L suppress circuit
- A CAMAC control section

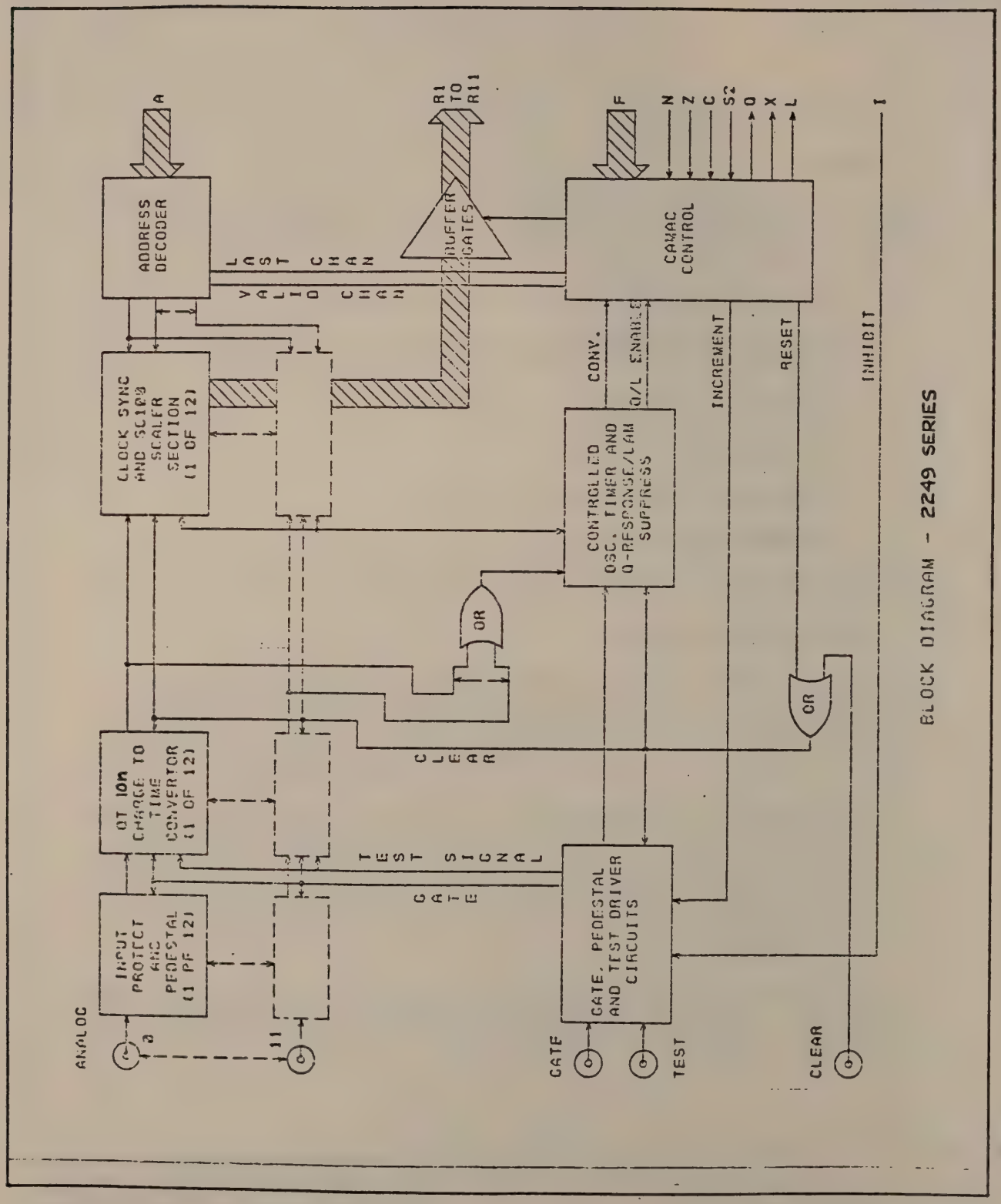
Separate descriptions of each of these circuit blocks follow.

5b. Charge-To-Time Converter

Each of the 12 inputs employs a hybrid charge-to-time converter (QTC). Specifications, block diagrams and waveforms for the QT100C are enclosed with this manual after the Functional Description section. The QTC consists of a virtual ground input amplifier, a linear gate driving a stable integrating capacitor, a current source, and an output differential amplifier.

The analog input of the 2249A and SG is a virtual ground with approximately 5 to 6 Ω impedance. It can be driven either from the front panel analog input via a 44 Ω resistor or from the common test input bus (which supplies each channel with an amount of charge proportional to the test input level supplied at the front panel or rear patch pin. (Without any TEST input, a high impedance connection to +12 volts generates an approximate 60% of full scale reading.)

*The QT100C and QT100B are identical and interchangeable. The letter change indicates only a change in method of manufacturing. These are used in the 2249A and SG. The QT102 is used in the 2249W and may not be interchanged with the QT100 series.


BLOCK DIAGRAM - 2249 SERIES
ADDRESS DECODER
A
R1 TO R11
BUFFER GATES
F
N
Z
C
S2
Q
X
L
CAMAC CONTROL
I
LAST CHAN
VALID CHAN
CONV.
G/L ENABLE
INCREMENT
RESET
INHIBIT
CLOCK SYNC AND SCALER SECTION (1 OF 12)
CONTROLLED OSC. TIMER AND Q-RESPONSE/LAM SUPPRESS
OR
OR
CLEAR
QT ION CHARGE TO TIME CONVERTOR (1 OF 12)
TEST SIGNAL
GATE
INPUT PROTECT AND PEDESTAL (1 PF 12)
GATE, PEDESTAL AND TEST DRIVER CIRCUITS
ANALOG
GATE
TEST
CLEAR

The front panel input has 44 Ω of resistance divided into two parts with input clamp diodes at their junctions to provide input protection and reduce crosstalk on large overloads. These resistors, in series with the low input resistance of the linear gate, terminate the input cable to 50 Ω. The stored charge is therefore $Q = \int_0^{Tg} (V_{in}/50\Omega)dt = \int_0^{Tg} i_{in} dt$, where V_{in} is the time dependent voltage on the analog input and Tg is the duration of the gate pulse. The current handling capability of the gate limits the linear range of the analog input to -20 mA (or -1.0 volts across the 50 Ω input).

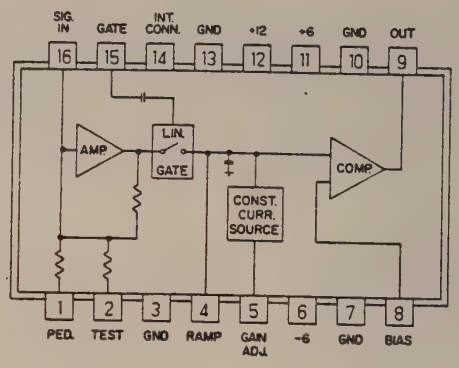
The required gate input signal is a standard NIM logic level, with recommended duration of 10 nsec minimum to 200 nsec maximum. The analog input is enabled for the duration of the gate.

The QT102 used in the 2249W employs a similar circuit, also with a 50 Ω input impedance. The input is, however, AC coupled via a 6.8 μF capacitor on the circuit board.

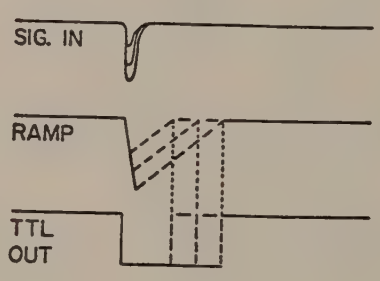
The charge delivered to the integrating capacitor through the linear gate is subsequently removed by means of a stable current source (see QTC Block and Waveform diagram). Thus, the voltage across the integrating capacitor is returned to its quiescent level at a constant rate. This rate is proportional to the difference between the +24 and V_{REF} inputs (Gain Adjust and +12 respectively, on block diagram). The output amplifier senses the voltage across this capacitor and generates an output level as long as this voltage is greater than a reference level (which is set by the 30 mV bias voltage). The output time duration (T) is therefore proportional to the input charge Q,where time T in microseconds is approximately 0.4 times the charge Q in picocoulombs (i.e., T = 0.4 Q μsec/pC). Operation of the QTC is assured by on-board stabilized ±5 V supplies, keeping a perfect balance in the QTC. The V_{REF} (approximately +12 VDC) tracks the +24 VDC supply, causing the difference (used as the current source reference) to be independent of external supply variations. A small fixed amount of charge is always put into the analog input when a gate pulse is generated. Each ADC channel has been factory calibrated to read between 1 and 2 pC (for gate pulse widths of 50 nsec) when all the inputs are externally loaded with 50 Ω terminations. If the inputs are not terminated, a slightly lower reading will be observed.

A Clear command can be used if desired to clear the 2249 during a conversion

LOGIC DIAGRAM (Top View)



INPUT-TO-OUTPUT WAVEFORMS



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cycle. It not only initializes all the digital control and scaler stages, but also, via a leading edge R-C differentiator, clears the analog ramp of the QTC to its quiescent level. The analog clear pulse width is about 300 nsec, leaving the 0.9 μsec remainder of the digital clear for settling in the QTC.

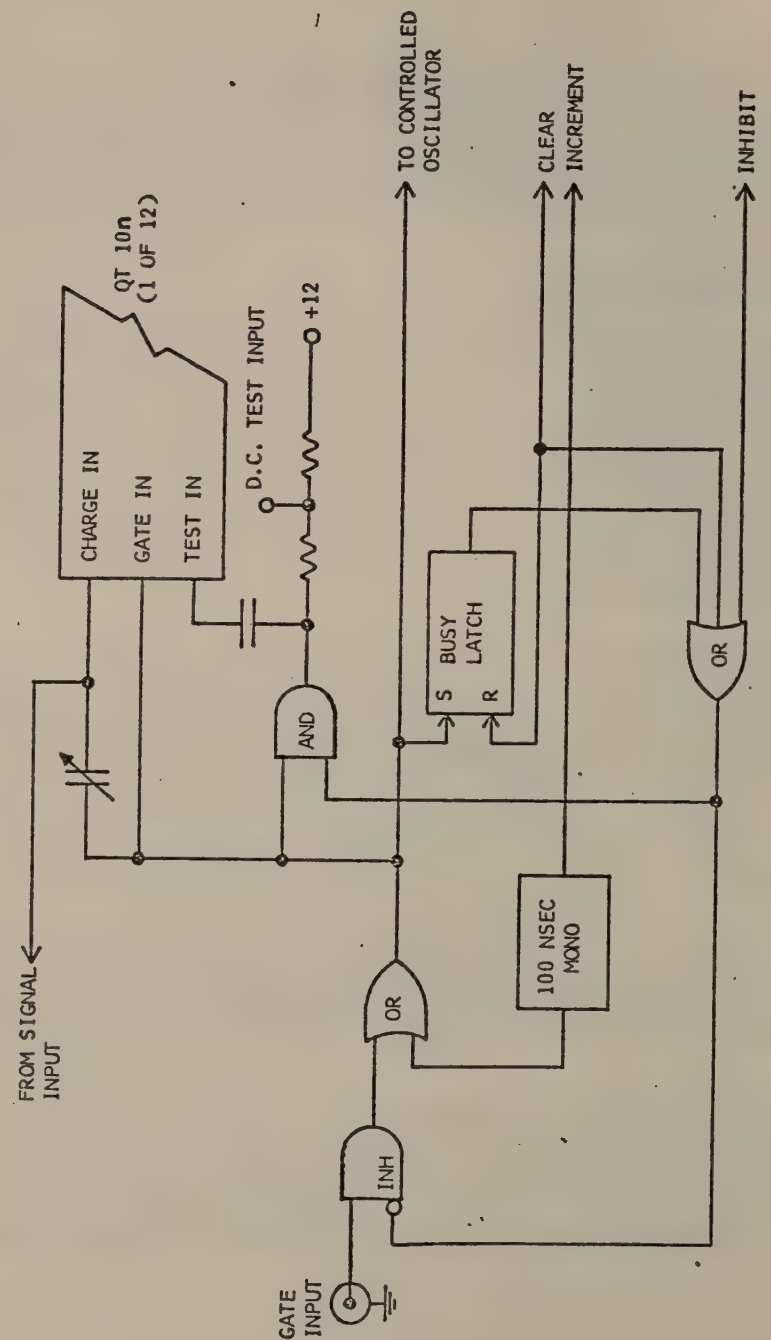
5c. Gate, Test and Pedestal Circuit

The gate generator is operated by either a front panel fast NIM input signal or by an increment signal supplied by the CAMAC controller. The internal gate pulse will actually enable the analog inputs of the A and SG versions about 4 nsec after application and the W version, 7 nsec after. It should, therefore, precede any input by at least that amount. The actual duration will be equal to the input plus about 4 nsec for the A and SG versions, 5 nsec for the W. The increment pulse supplied by the CAMAC control section generates a 100 nsec wide gate pulse (see schematic, sheet 3, and block diagram) upon application of an F(25). Its action is to enable the gate and generate a test pulse.

The test input of the 2249A and W is connected through a precision resistor to a common capacitor C Test in the test circuit. The charge which is stored in this capacitor is equally shared by all channels. The CAMAC Inhibit must be used when testing the unit with F(25). On an INRC command (F(25)·S2), the CAMAC control generates a pulse width 100 nsec which is OR'd into the gate circuit. In addition, if an inhibit condition exists, INCR discharges the test capacitor equally into the 12 QTC's during the 100 nsec gating interval. The test input accepts a positive DC level of 0 to 20 volts to produce a zero to full scale digital output of each ADC.

The trailing edge of the output of the gate generator also produces an initiate pulse which is used to set the busy latch and generates the delayed pulse which starts the conversion cycle. The busy latch feeds back to inhibit the gate within 100 nsec of the trailing edge and is cleared by the reset pulse.

The pedestal is adjusted by injecting charge via a trimmer capacitor (C_{PED}) into the virtual ground of the QTC from the leading edge of the gate pulse where the amount of charge is proportional to the C_{PED} in pFd times the voltage swing of the gate pulse. The trailing edge of the gate is not coupled in because the gate closes and blocks the charge. Because of the



BLOCK DIAGRAM - GATE, PEDESTAL, TEST CIRCUIT

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

charge injection time constant, gate widths narrower than 50 nsec (500 nsec) will not allow all of the injected pedestal charge to be accumulated by the 2249A (2249W). This causes a reduction of the pedestal reading somewhat faster than indicated by the gate dependent term in the specifications.

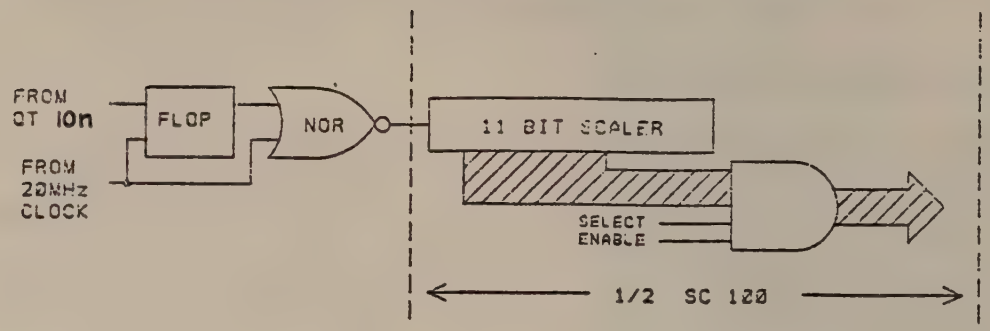
5d. Clock Synchronizer and Scaler

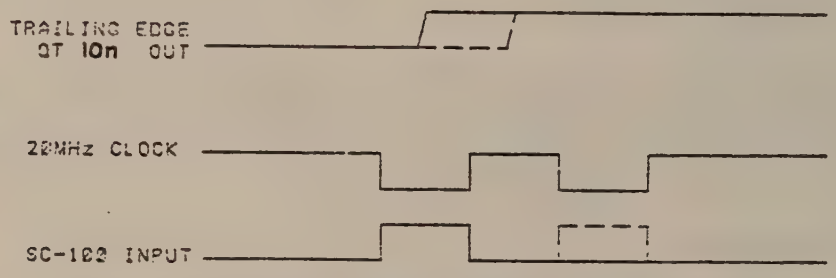
The output of each QTC hybrid in the 2249 Series is used to gate an oscillator into one half of a LeCroy hybrid SC100 Dual Eleven-Bit Scaler. The Oscillator is synchronously started with respect to the leading edge of the gate (see Controlled Oscillator section). This ensures no fractional pulses during the beginning of the rundown cycle, but care must be taken at the end of the rundown. This is done by the synchronizing stage. Each gate circuit (see schematic sheet 2, and block diagram) supplies an integral number of clock pulses even if the QTC output returns to its quiescent state in the middle of a clock pulse as shown in the previous diagram.

When the conversion cycle is complete, readout of the addressed scaler can be done by enabling the proper SC100 (using decoded A2, A4, and A8 subaddress lines) and selecting the proper half of the SC100 (using the A1 subaddress). Along with F(0) or F(2) and N, the 11-bit data will be gated out in parallel to the CAMAC dataway.

5e. Controlled Oscillator

The clock circuit is a modified Colpitts oscillator employing a highly temperature stable choke and a mica capacitor as its resonant elements. Its frequency is 20MHz. The oscillator is gated on 2.2 μsec after the leading edge of the gate pulse. Gating the oscillator in this way eliminates the uncertainty of one count associated with an asynchronous oscillator and eliminates noise and nonlinearities caused by not delaying the turn-on (see block diagram). The conversion time is set to 60 or 105 μsec allowing more than enough time for the nominal 50 μsec or 100 μsec full scale conversion to occur for the 2249A and SG or W, respectively. This allows for the ±5% differences from channel to channel, slight temperature drifts, module to module variations, etc., and still ensuring that an overflow can occur for oversized input pulses.





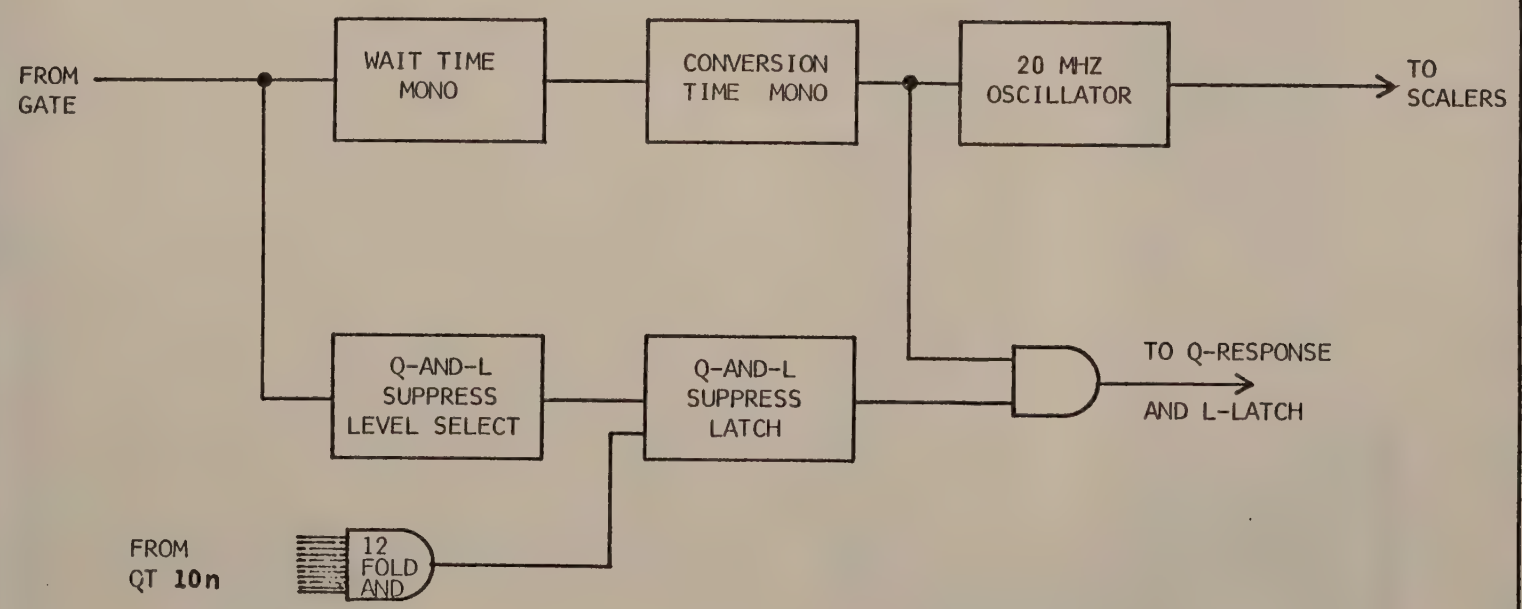
BLOCK DIAGRAM - CLOCK SYNC AND SCALER

5f. LAM and Q-Response Suppress Circuit

At the beginning of the gate pulse, a monostable is set (see block diagram). The RC time constant of this monostable is adjustable by a side panel potentiometer labeled Q and L SUPPRESS LEVEL ADJUST. When the monostable resets, a latch is reset if one or more of the QTC outputs is still on. If set, this latch disables the Q-response circuit (that normally indicates valid data on an F(0) or F(2) Read Command) and clears the LAM latch. Disabling of the suppress function can be done for either Q-response or L. See the Operational section for more information.

5g. The CAMAC Control

The decoding of the CAMAC "F" functions and N is performed by a 4 line to 16 line decoder (an SN74154). A DC level is generated at the appropriate pin for each valid CAMAC command. Scaler addressing is accomplished using a 4 line to 10 line decoder (an SN7442) on A2, A4, and A8, to enable the appropriate SC100 20 channel scaler hybrid and the A1 bit is used to select the appropriate half of the SC100. X-response is generated for all valid commands, and Q-response and LAM are generated as described in the Q and L Suppress Circuit section.



BLOCK DIAGRAM - CONTROLLED OSCILLATOR AND Q-RESPONSE AND L SUPPRESS

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

technical information manual

ME 8255

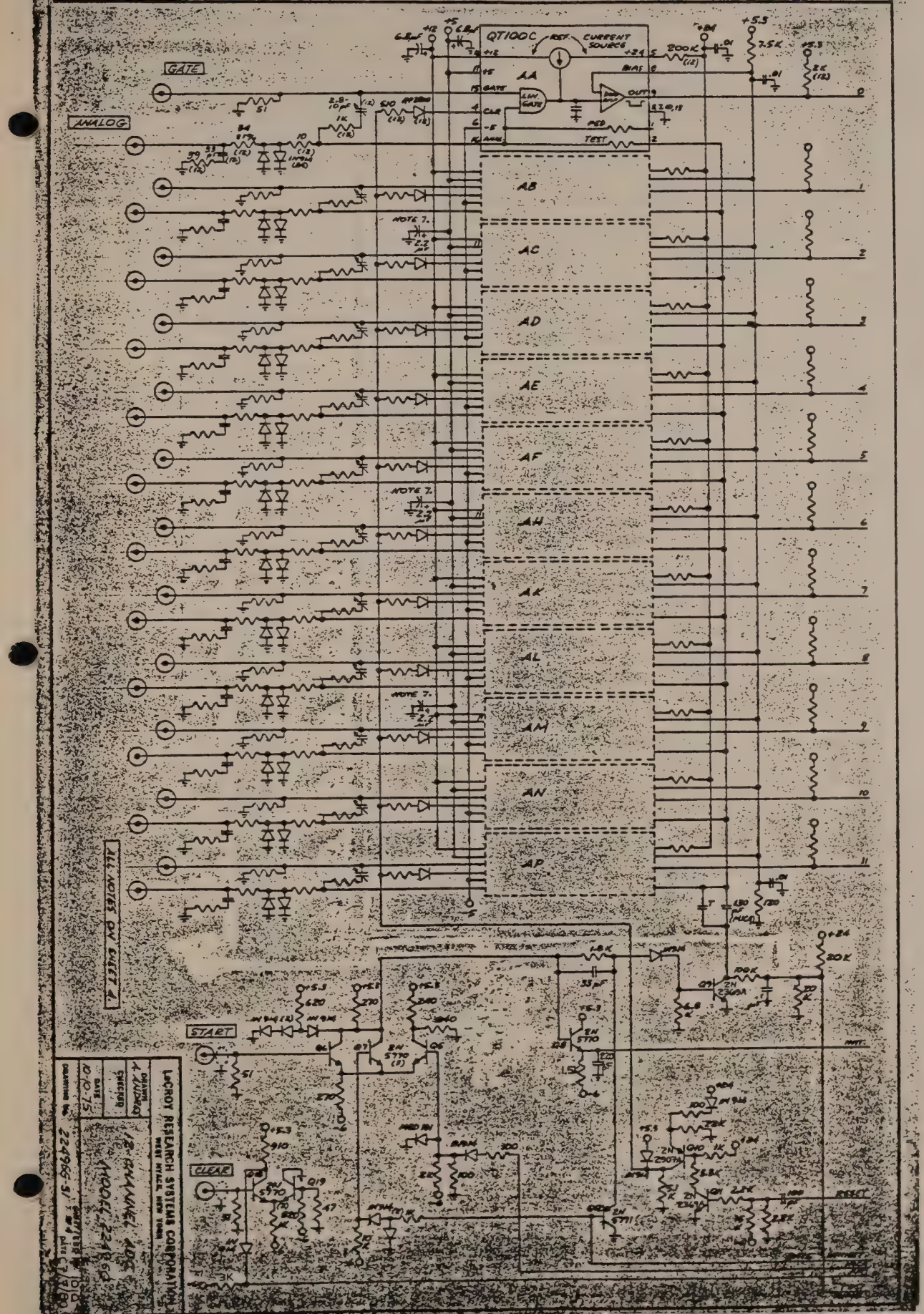
MODEL NO 2249SG 12-CHANNEL ADC PRINTED 10-Apr-81
LAST REVISION NO 1010 REVISION DATE 07-Jul-80

168	531	454	RES PREC RN55D	4.32 K	1
168	531	461	RES PREC RN55D	5.11 K	2
181	457	501	RES VARI CERMET	500 OHMS 1/2W 10%	3
181	457	503	RES VARI CERMET	50 K 1/2W 10%	1
200	*31	**1	IC 2-IN NAND GATE	SN7400N QUAD PKG/DIP-14	2
200	*31	**2	IC 2-IN NAND GATE	SN7401N QUAD PKG/DIP-14/OPEN COLLECTOR	4
200	*31	**3	IC 2-IN NOR GATE	SN7402N QUAD PKG/DIP-14	6
200	*31	**4	IC HEX INVERTER	SN7404N DIP-14	2
200	*31	**7	IC 3-IN NAND GATE	SN7410N TRIPLE PKG/DIP-14	1
200	*31	**9	IC 8-IN NAND GATE	SN7430N SINGLE PKG/DIP-14	1
200	*31	*11	IC J-K M-S FL-FL	SN7473N DUAL PKG/DIP-14	1
200	*31	*30	IC FLIP-FLOP	SN7474N DUAL D-TYPE EDGE-TRIGGERED/DIP-14	7
200	*41	**1	IC DECODER	SN7442N 4-LINE-TO-10-LINE/DIP-16	1
200	*42	**2	IC MULTIVIBRATOR	9602PC DUAL RESETTABLE MONOSTABLE/DIP-16	2
200	*81	**4	IC DECODER/DEM	DM74LS154N DIP-24	1
208	*11	**3	IC SINGLE OP AMP	LM301AN DIP-8	3
210	*40	*13	IC CHG-TO-TIME CON	QT100C DIP-16	12
210	*80	**1	IC 11-BIT SCALER	SC100 DUAL PKG/DIP-24	6
230	110	**5	DIODE SWITCHING	1N4448	39
235	*50	**1	DIODE RECTIFIER	1N4139	1
240	225	705	DIODE ZENER 4.85V	1N705A 250MW	3
240	225	710	DIODE ZENER 6.8V	1N710A 250MW	1
253	*10	800	DIODE HOT CARRIER	HP2800 V BR 70V/H-P CASE 15	12
253	*10	835	DIODE HOT CARRIER	HP2835 H-P CASE 15	1
270	110	**1	TRANSISTOR NPN	2N2369A TO-18	2
270	150	**1	TRANSISTOR NPN	2N3053 TO-5	2
270	170	**1	TRANSISTOR NPN	2N5770 TO-92	11
275	110	**1	TRANSISTOR PNP	2N2907A TO-18	1
275	150	**3	TRANSISTOR PNP	40319 TO-5	1
275	170	**2	TRANSISTOR PNP	2N5771 TO-92 SEE 275-170-004(MPS3640)	15
300	*50	**1	CHOKE FERRITE SINGLE LEAD		4
302	**0	**1	INDUCTOR SPECIAL	1.00 UH	1
400	*10	**8	SOCKET IC ST	DIP-8 BONDED TIN CONTACTS/COPP-NICKEL PINS	3
400	*20	*14	SOCKET IC ST	DIP-14 BONDED TIN CONTACTS/COPP-NICKEL PINS	24
400	*30	*16	SOCKET IC ST	DIP-16 BONDED TIN CONTACTS/COPP-NICKEL PINS	15
400	*40	*24	SOCKET IC ST	DIP-24 BONDED TIN CONTACTS/COPP-NICKEL PINS	7
402	*30	**0	CONNECTOR CO-AXIAL	LEMO	27
402	*30	**1	HOOD FOR BULKHD LEMO CONN	LEMO CR00.001.250	2
402	*30	**2	SPANNER NUT SMALL OD	LEMO	27
402	*30	**3	GROUND LUG NONLOCK	LEMO	A/R
402	*30	**4	GROUND STRAP 'H'	LEMO	A/R
433	220	**2	FUSE SUB-MINI	3 AMP	2
540	203	**1	SIDE COVER CAMAC STD	(LIP)	1
540	206	**1	RAIL	CAMAC STANDARD	2
540	209	**2	REAR PANEL	CAMAC SIZE *2	1
555	430	**3	CAPTIVE SCREW ASSEMBLY		1
712	249	*23	PC BD PREASS'Y	2249SG	1
722	249	*23	FRONT PNL PREASS'Y	2249SG 54020200 2(1)	1
732	249	*13	SIDE CAMAC LEFT	2249A 54020300 1(1)	1

NOTES 1
NOTES 2
NOTES 3
NOTES 4

MODEL NO 2249SG 12-CHANNEL ADC PRINTED 10-Apr-81
LAST REVISION NO 1010 REVISION DATE 07-Jul-80

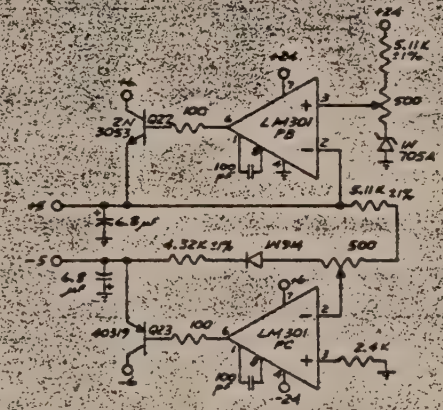
101 246 **2	PC STOCK DBL SIDED	1 OZ		119M
102 145 104	CAP CERA DISC 12V	.1 UF	PT-FDCL-1/32 LEADS 3/8 AWG 22	3
102 245 103	CAP CERA DISC 25V	.01 UF	PT-FDCL-1/32 LEADS 3/8 AWG 22	15
102 444 101	CAP CERA DISC 100V	100 PF	10% S3N	4
102 444 330	CAP CERA DISC 100V	33 PF	10% S2L	13
102 745 221	CAP CERA DISC 500V	220 PF	PT-FDCL-1/32 LEADS 3/8 AWG 22	1
116 **0 910	CAP DIP MICA SPECL	91 PF	5% TC: 0 TO +70 PPM/C	2
116 515 131	CAP DIP MICA DM10	130 PF		1
116 515 151	CAP DIP MICA DM10	150 PF		1
116 515 241	CAP DIP MICA DM10	240 PF		1
116 525 681	CAP DIP MICA DM15	680 PF		1
125 535 103	CAP POLYCARB FILM	.01 UF	50V 5%	1
141 494 225	CAP TANT (MINI)	2.2 UF	'NON-CORROSIVE' CASE/RADIAL LEADS	5
142 824 685	CAP TANT DIP CASE	6.8 UF	35V 20%	10
147 147 *90	CAP ALUM METAL CAN	90 UF	6V -10% +75%	2
158 819 **1	CAP VARI CERA	3.5 - 18 PF		2
158 819 **2	CAP VARI CERA	3.0 - 10 PF		12
161 335 100	RES COMP 1/4W 5%	10 OHMS		12
161 335 101	RES COMP 1/4W 5%	100 OHMS		6
161 335 102	RES COMP 1/4W 5%	1 K		20
161 335 103	RES COMP 1/4W 5%	10 K		4
161 335 104	RES COMP 1/4W 5%	100 K		1
161 335 121	RES COMP 1/4W 5%	120 OHMS		1
161 335 122	RES COMP 1/4W 5%	1.2 K		1
161 335 152	RES COMP 1/4W 5%	1.5 K		1
161 335 153	RES COMP 1/4W 5%	15 K		1
161 335 182	RES COMP 1/4W 5%	1.8 K		1
161 335 202	RES COMP 1/4W 5%	2 K		15
161 335 203	RES COMP 1/4W 5%	20 K		4
161 335 204	RES COMP 1/4W 5%	200 K		12
161 335 222	RES COMP 1/4W 5%	2.2 K		4
161 335 223	RES COMP 1/4W 5%	22 K		1
161 335 241	RES COMP 1/4W 5%	240 OHMS		2
161 335 242	RES COMP 1/4W 5%	2.4 K		1
161 335 243	RES COMP 1/4W 5%	24 K		1
161 335 271	RES COMP 1/4W 5%	270 OHMS		2
161 335 273	RES COMP 1/4W 5%	27 K		1
161 335 302	RES COMP 1/4W 5%	3 K		2
161 335 332	RES COMP 1/4W 5%	3.3 K		2
161 335 390	RES COMP 1/4W 5%	39 OHMS		12
161 335 392	RES COMP 1/4W 5%	3.9 K		1
161 335 470	RES COMP 1/4W 5%	47 OHMS		1
161 335 472	RES COMP 1/4W 5%	4.7 K		2
161 335 510	RES COMP 1/4W 5%	51 OHMS		14
161 335 511	RES COMP 1/4W 5%	510 OHMS		13
161 335 512	RES COMP 1/4W 5%	5.1 K		2
161 335 621	RES COMP 1/4W 5%	620 OHMS		1
161 335 682	RES COMP 1/4W 5%	6.8 K		2
161 335 752	RES COMP 1/4W 5%	7.5 K		2
161 335 820	RES COMP 1/4W 5%	82 OHMS		2
161 335 821	RES COMP 1/4W 5%	820 OHMS		1
161 335 911	RES COMP 1/4W 5%	910 OHMS		1
161 555 151	RES COMP 1W 5%	150 OHMS		1
168 531 252	RES PREC RN55D	34.0 OHMS		12

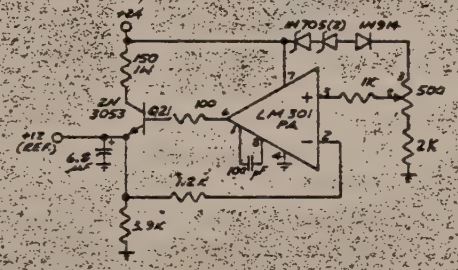

QT100C
REF. CURRENT SOURCE
GATE
ANALOG
AA
AB
AC
AD
AE
AF
AH
AK
AL
AM
AN
AP
ALL NOTES ON SHEET 4
START
CLEAR
RESET
LECROY RESEARCH SYSTEMS CORPORATION
DRAWN
CHECKED
DATE
10-10-75
DRAWING No.
224965-51
MODEL 2249 SG
12-CHANNEL ADC

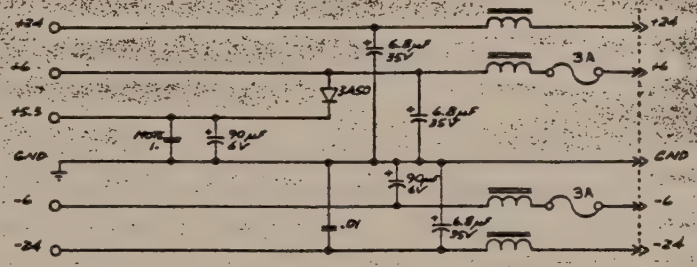
LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK
12-CHANNEL ADC
MODEL 2249 SG
DRAWING No. 2249SG-S1
DRAWN A. ANDRES
CHECKED
DATE 10-10-75
SHEET 1 OF 4 DWG
ALL NOTES ON SHEET 4
INIT
RESET
GATE INHIBIT
TEST INPUT
COMP.
GEN
T.P.
DA
DC
DE
DG
DH
DK
DL
DN
BA
BC
BE
BF
BH
BK
BL
BN
SC100 (NOTE 2) (4)
SN7402
SN7474 (6)
2N5770
2N5771
SN7410
SN74LS74
TD 9602 (60 μs)
TC 9602 (2-10 μs)
GATE INHIBIT
TEST INPUT

READ
E01
E23
E45
E67
E89
E1011
RESET
CONV.
GEN
RESET
INH.
INCR. PTC
TEST INPUT
ALL NOTES ON SHEET 4.
SN7442
SN7400
SN7402
SN7404
SN7401
74LS154
SN7410
SN7473
SN74123
JUMPER IC OPTION
150 pF (MICA)
2.2K
4.7K
20K
240pF (MICA)
1K
1N916
A2
A1
A0
FA
FB
FC
FD
FE
X
Q
Z
C
S2
N
LAM
P1
P2
P3
P4
LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK
DRAWN A. MUSKUS
CHECKED
DATE 10-10-75
12-CHANNEL ADC
MODEL 2249 SG
DRAWING No. 2249SG-51
SHEET 3 OF 4 DWG. REV. 10/10/75

I.C.	REFERENCE	+24V	+12V	+6V	+5.3V	+5V	GND	-24V
301	FC			7				4
501	FA, FB	7					4	
DM8093	AL, AB, AK, AD, AJ, AF, AH, AE, AA, AM, AN, AP	8	12			11	3,9,10,13	
8200	BA, BC, BE, BG, BJ, BK				1		2	
DM7400	FD, FE				14		7	
7401	RA, RB, RC, SA				14		7	
7402	CA, CB, CH, CK, SF, TF				14		7	
7404	SL, TK				14		7	
7420	TH				14		7	
7432	SA				14		7	
7442	SK				16		8	
7473	SC				4		11	
7474	RA, RC, RF, RK, RL, TB				14		7	
74LS160	SB				24		12	
9602	TC, TD				16		8	







NOTES:

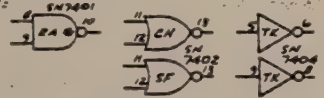
1). ADDITIONAL .01µF CERAMIC CAPACITORS ON +5.3 VOLT BUS, NOT SHOWN.

2). ALL 9200-s ARE WIRE OR-ED.

3). "T" DESIGNATES VALUE TO BE CHOSEN AT TEST.

4). * DENOTES OPEN COLLECTOR.

5). UNUSED GATES:



6). ALL IN914 DIODES MAY BE REPLACED BY IN 4148 OR IN 4448.

7). 2.2µF CAPACITOR, ACROSS PINS 3 TO 11, THREE PLACES.

LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

DRAWN: A. ANDRES
CHECKED:
DATE: 10-10-75

12- CHANNEL ADC
MODEL 2249SG

DRAWING No. 2249SG-51 SHEET 4 OF 4 REV. 1010
DATE 11/1/80

STATUS INFORMATION

Status information is conveyed by signals on the Look-at-Me (L), Busy (B), and Response (Q) lines.

Look-at-Me (L)

This, like the N line, is an individual connection from each station to a separate pin at the control station. When there is no Dataway operation in progress (no B present) any plug-in unit may generate a signal on its L line to indicate that it requires attention. When B is present each L signal is gated off the Dataway line by the unit which generates it.

A Look-at-Me request can be reset by Clear Look-at-Me, Initialize, or by the performance of the specific action which generated the request.

Dataway Busy (B)

The Busy signal is used to interlock various aspects of a system which can compete for the use of the Dataway. Specifically, it is generated during Dataway command or common control operations. Whenever N is present, B is present, and for the duration of B, all L signals are gated off the Dataway lines.

Response (Q)

The Q bus-line is used during a Dataway operation to transmit a signal indicating the status of a selected feature of the module.

On all Read and Write commands the signal on the Q bus-line remains static from the time the command is received until S2. For all other commands the signal on the Q bus-line may change at any time.

COMMON CONTROLS

Common control signals operate on all modules connected to them, without requiring to be addressed by a command. In order to provide protection against spurious signals the Initialize (Z) and Clear (C) signals must be accompanied by Strobe S2.

Initialize (Z)

The Initiallze signal has obsolute priority over all other signals or controls. It sets all units to a basic state by resetting all resetting all registers, whether data or control, to a defined state, and by resetting all L signals and disabling them where possible. Units which generate must also cause S2 and B to be generated. Modules which accept Z gate it with S2 as a protection against spurious signals on the Z line.

Inhibit (I)

The presence of this signal inhibits any activity (for example, data taking). It must either not change when B is present or have rise and fall times not less than 200 ns.

Clear (C)

This common signal clears all registers or bistables connected to it. Units which generate C must also cause S2 and 3 to be generated. Modules which accept C gate it with S2 as a protection against spurious signals on the C line.

PRIVATE WIRING

Patch Leads (P1-P7)

Five pins (P1 to P5) on the 86-way socket at normal stations are not prewired to Dataway lines but are freely available for local connections. At the control station seven pins (P1-P7) are available. Signals on the patch pins must either remain static when B is present or have rise and fall times not less than 20 ns.

DATAWAY COMMAND OPERATIONS

A command is composed of signals on the Station Number line or lines, the Sub-Address lines and the Function lines. It is accompanied by a signal on the Busy Line. In response to a command, data may be transferred on the Read or Write lines and one bit of status information on the Q line. The two Strobes S1 and S2 must be generated in each Dataway command operation and control its timing.

The order in which the commands are described below corresponds to the function codes set out in Table 2. In this table the term 'register' is used for an addressable data source or receiver, without implying that it has a data storage property. The function codes allow the registers in a module to be divided into two distinct sets, known as Group 1 and Group 2. Thus it is possible to operate on more than the basic set of 16 registers selected by the 4 sub-address lines.

A common feature of all commands is that if the module has a Look-at-Me source which requests a specific command then the performance of that command should be reset the Look-at-Me source.

Read Commands (Function Codes 0-7)

Read commands are identified by the combination F16 = 0, F8 = 0 in the function code. They specify that information is to be transferred from a module to a controller via the R bus-lines. Data signals are set up on the R bus-lines by the module as soon as the 'Read' command is recognized, and the appropriate status signal connected to the Q bus-line. The R and Q signals reach a steady state before S1, and are maintained for the full duration of the Dataway command operation unless the state of the signal source is changed at S2. The controller or other common data receiver strobes the data from the R and Q bus lines at the time of the strobe S1.

In order to facilitate reading by sequential addressing, all registers containing data (as opposed to control information) must have cosecutive sub-addresses starting at sub-address 0. At each of these sub-addresses the module generates Q = 1 in response to the appropriate Read command. At the next sub-address in sequence (where there is not a data register) the response is Q = 0. At all remaining sub-addresses the Q signal may be used to test any feature, subject to the general requirement that the Q signal must be static from the beginning of command until at least S2.

Code 0, Read Group 1 Register

This command selects, by sub-address, one register from the first group in the module and transfers the contents of this register to the controller. The contents of the register remain unchanged.

Code 1, Read Group 2 Register

Same as Code 0, except command selects register from the second group.

Code 2, Read and Clear Group 1 Register

Same as Code 0, except the module register is cleared at time S2.

Code 3, Read Complement of Group 1 Register

Same as Code 0, except command transfers the complement of the contents of this register to the controller.

Code 4 - 7

Unassigned at this time.

CONTROL COMMANDS (Function Codes 8 - 15)

Control commands are identified generally by F8 = 1 in the function code. They are divided into two groups by the state of F16, in this case F16 = 0. They specify that information is not transferred on either the R or W bus-lines. However, information may be conveyed on the Q bus-line in any of these commands. The signal on the Q bus-line may change at any time but is strobed into the controller at time S1 and may (except in Code 8) be reset by strobe 2.

Code 8, Test Look-at-Me

This command selects a Look-at-Me source in the module and presents the state of this source on the Q bus-line.

Code 9, Clear Group 1 Register

This command selects, by sub-address, a register from the first group in the module and clears the contents of this register.

Code 10, Clear Look-at-Me

Same as Code 8, except the Look-at-Me source is cleared at time S2.

Code 11, Clear Group 2 Register

Same as Code 9, except command selects register from the second group.

Code 12-15

Unassigned at this time.

WRITE COMMANDS (Function Codes 16-23)

Write commands are identified by the combination F16 = 1, F8 = 0 in the function code. They specify that information is to be transferred from a controller to a module via the W bus-lines. The controller or other common data source generates data signals on the W bus-lines at the beginning of the "Write" operation. The module connects the appropriate status signal to the Q bus-line as soon as the command is recognized. The W and Q signals reach a steady state before S1 and are maintained for the full duration of the Dataway command operation unless the status of the signal source is changed at Strobe 2. In order to facilitate writing into registers by sequential addressing, all registers which are to contain data (as opposed to control information) have consecutive sub-addresses starting at sub-address 0. At each of these sub-addresses the module generates Q = 1 in response to the appropriate Write function. At the next sub-address in sequence (where there is not a data register) the response is Q = 0. At all remaining sub-addresses the Q signal may be used to test any feature subject to the general requirement that the Q signal must be static from the beginning of the command until at least S2.

Code 16, Overwrite Group 1 Register

This command selects, by sub-address, one register in the first group in the module and sets the contents of this register to correspond with the data generated on the W bus-lines by the controller.

Code 17, Overwrite Group 2 Register

Same as Code 16, except command selects register in the second group.

Code 18, Selective Overwrite Group 1 Register

Same as Code 16, except a separate "mask" register defines which bits in the selected register are set.

Code 19, Selective Overwrite Group 2 Register

Same as Code 18, except command selects register in the second group.

Code 20 - 23

Unassigned at this time.

CONTROL COMMANDS (Function Codes 24 - 31)

Control commands are identified generally by F8 = 1 in the function code. They are divided into two groups by the state of F16, in this case F16 = 1. They specify that information is not transferred on either the R or W bus-lines. However, information may be conveyed by the Q bus-line in any of these commands. The signal on the Q bus-line is permitted to change at any time but is strobed into the controller at time S1 and may (except in Code 27) be reset by strobe S2. Precautions must be taken to ensure that information is not lost due to Q signals appearing between S1 and S2.

Code 24, Disable

This command selects, by sub-address, and disables a feature of the module; e.g., a Look-at-Me source or a data input.

Code 25, Increment Preselected Registers

This command adds one simultaneously to the contents of each register in one of 16 groups, defined by the sub-address.

Code 26, Enable

This command enables the feature of the module selected by the sub-address, e.g., a Look-at-Me source or a data input.

Code 27, Test Status

This command selects, by sub-address, any feature of a module other than a source of a Look-at-Me request, and tests it by producing a response on the Q bus-line.

Code 28 - 31

Unassigned at this time.

DIGITAL SIGNAL STANDARDS ON THE DATAWAY

The potentials for the binary digital signals on the Dataway lines have been defined to correspond with those for compatible current sinking logic devices (e.g., the TTL and DTL series). The signal convention has, however, been inverted to be negative logic. The high state (more positive potential) corresponds to logic '0' and the low state (near ground potential) corresponds to logic '1'. Intrinsic OR outputs are thus available from the manufacturers' standard product range, and disconnected inputs go to the '0' state.

It is an essential feature of the Dataway that many units may have their signal outputs connected to the Read and Response lines. Outputs onto these lines therefore require intrinsic OR gates. The same principle is extended to other lines (Command, Write, etc.) in order to allow more than one controller-like unit in a crate. The Inhibit line may be an exception, since its signals are shaped with a slow rise and fall if they change during Dataway operations.

Voltage standards for Dataway Signals

All Dataway Signals must conform to the voltage levels as follows:

Pull-up current sources for all Dataway bus-lines are located in the crate controller (occupying the control station and at least one other station) so as to insure that there is one and only one current source per line. The minimum pull-up current when the Dataway line is at +3.5 V is defined in Table 4 as 2.5 mA but, if the controller generates Dataway signals at time intervals near the permitted minima, the pull-up current sources should preferably provide not less than 6 mA when the lines are at this potential. The pull-up for the N signals is located in the unit generating the signals and for the L signals in the unit receiving the signals so that the individual lines may be joined or grouped within these units if desired.

The N and L lines are effectively individual lines joining two units (a module and a controller) together. The Q and R lines will generally have many units generating the signals (say 20) with a few units (maximum 4) receiving the signals. The remaining lines (W, A, F, S, B, Z, I, C) will have relatively few units generating each signal (often only one) with the possibility of many units receiving the signals.

Timing of Dataway Signals

The sequence of events during a single Dataway operation is shown in Timing Diagram, Page 13C, by means of simplified signal waveforms. The shaded areas indicate the permitted variation of each signal between an ideal square signal and a signal whose transition across the appropriate signal threshold (0.8 V or 2.0 V) satisfies the conditions shown. The signal waveforms for the command and data lines apply to those lines, if any, which take up the '1' state. Other command and data lines may, of course, be in the '0' state during the operation.

The signals on the Busy line and the various signals constituting the command need not occur in exact synchroism, provided their envelope lies within the shaded areas of the diagram. Similar variation is permitted between the signals constituting the data. The broken line indicates the earlies time at which the data signals may change in response to S2.

Key points on these waveforms are indicated by t_0 - t_9, with the following significance:

Points t_0, t_3, t_6 represent the initiation of the negative-going of the Command, Strobe 1, and Strobe 2 signals, respectively. They are the times at which the signals would be received from an ideal Dataway with no capacitative loading.

Points t_9, t_5, t_8 represent similarly the initiation of the positive-going edges of the same signals.

Points t_2, t_{11} are the latest times at which the data source is permitted to initiate the negative-going and positive-going edges of the data signals.

Points t_1, t_3, t_4, t_7 represent the latest times at which the received signals are permitted to reach a maintained '1' state, and therefore refer to the last negative-going transition across the + 0.8 V threshold.

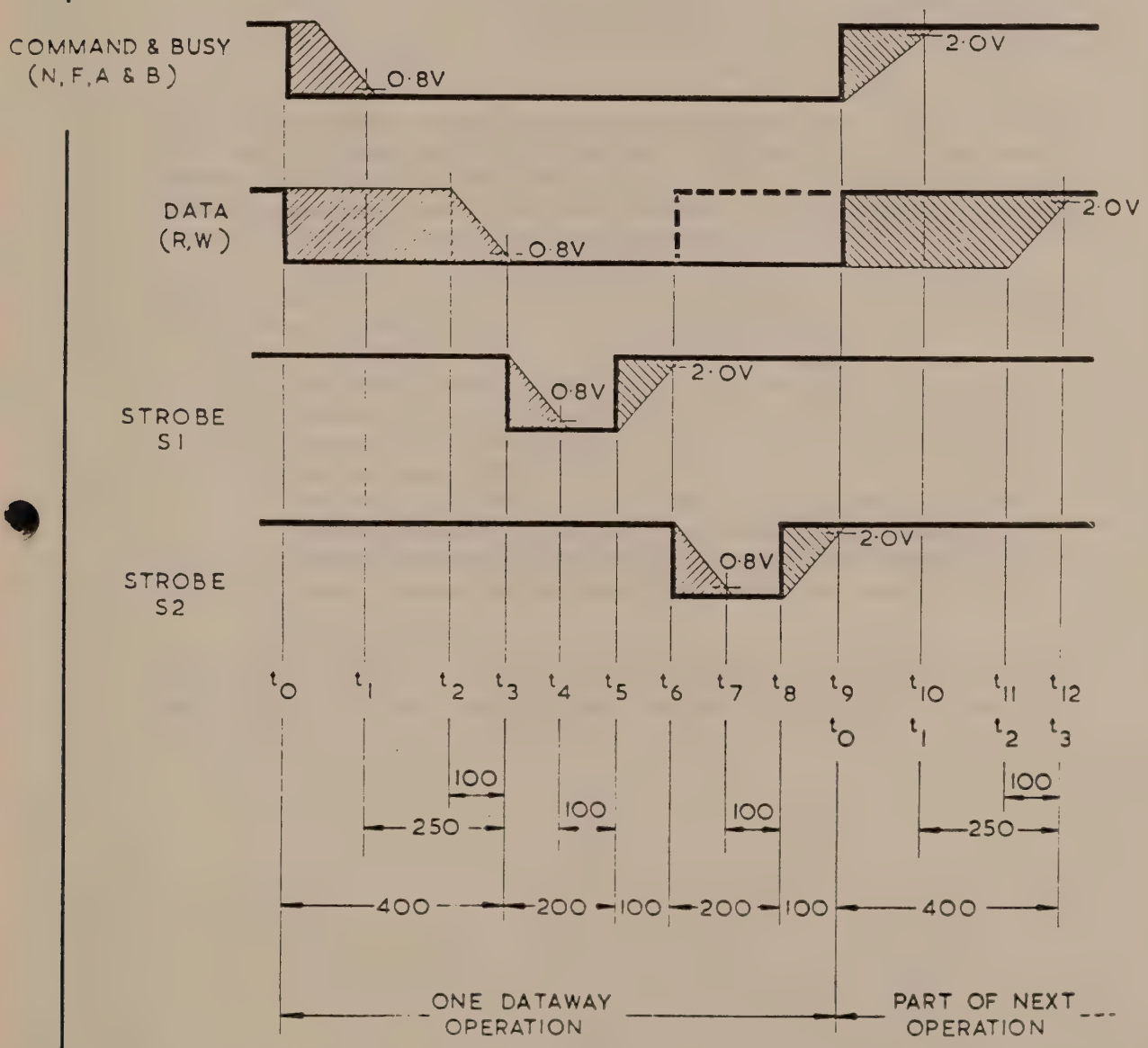
Points t_6, t_9, t_{10}, t_{12} represent the latest times at which the received signals are permitted to reach a maintained '0' state, and therefore refer to the last positive-going transition across the + 2.0 V threshold.

Controllers must initiate the negative and positive going edges of the command and strobe signals at intervals not less than those defined by t_3, t_5, t_6, t_8 and t_9. Modules respond to the command within the most adverse value of $(t_1 - t_2)$; i.e., 100 ns. The electrical characteristics of the Dataway and connections from it into units must allow signals to rise and fall within the minimum times for $(t_0 - t_1)$, $(t_2 - t_3)$ etc.

The next Dataway operation must not start before t_9.

The extreme case is shown in Timing Diagram, Page 15C, with the next operation starting at t_9, so that $t_9 - t_{12}$ of one operation coincide with $t_0 - t_3$ of the next. The command and data signals of one operation may thus be removed while those of the next operation are being established. The Busy signal may be maintained continuously during a sequence of consecutive Dataway operations. Under suitable conditions any command or data signals of one operation may thus be removed while those of the next operation are being established. The Busy signal may be maintained continuously during a sequence of consecutive Dataway operations. Under suitable conditions any command or data signals which have the same state during successive operations may also be maintained. In the extreme case of successive operations with the same command and data there could be a complete absence of signal transitions between t_0 and t_3.

DATAWAY TIMING



TIMES GIVEN ARE MINIMUM VALUES IN NANOSECONDS

TIMING OF A DATAWAY OPERATION.

POWER SUPPLIES

The voltage tolerances and current loadings are specified below. The specified tolerances in voltage refer to the voltage measured at the contacts of the Dataway sockets and must be maintained under the worst combination of factors such as a.c. mains voltages and frequency, the maximum current loadings, temperature and the position in the crate of the socket under observation.

Note that the maximum currents stated in the below table are subject to the over-all restrictions as follows:

1. The current carried by any contact of the Dataway socket must not exceed 3 A.
2. The total power dissipated in a crate, without forced ventilation, must not exceed 200 W.
3. The power dissipation per single width station should not, therefore, normally exceed 8 W; however, under special circumstances this rating may be increased to a maximum of 25 W provided suitable precautions are taken to comply with total power dissipation and current loadings.

The resistance between any point on the Dataway OV power return bus-line and the point at which the power supply is joined to the crate wiring must not exceed 2 milliohms.

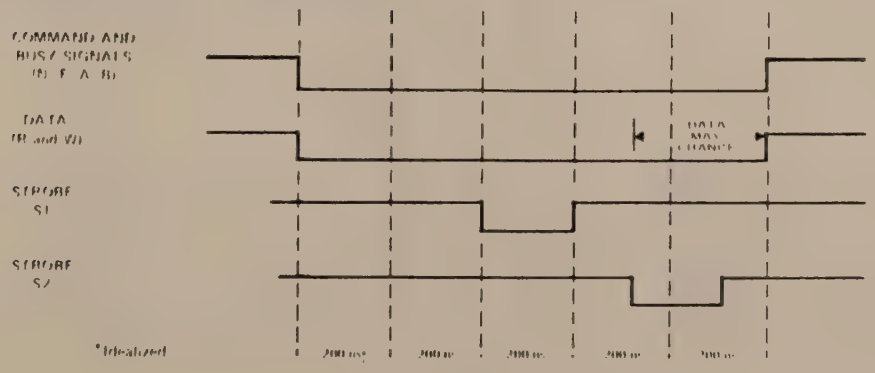
Supply Voltage	Voltage Tolerance	Maximum Current Loads	
		In the Plug-in (per unit width) See Notes (1) & (3) Above	In the crate See Note (2) Above
Mandatory			
+24V d.c.	± 0.5%	1A	6A
+ 6V d.c.	±2.5%	2A	25A
- 6V d.c	±2.5%	2A	25A
-24V d.c	±0.5%	1A	6A
OV			
Additional (as required)			
+200V d.c.	+60V, -20V		0.1A
+ 12V d.c.	± 0.5%		
- 12V d.c.	± 0.5%		
117V a.c.	+10%, -12%		0.5A

CAMAC Reference Data

CAMAC FUNCTION CODES

CODE F( )	FUNCTION	FUNCTION SIGNALS F16	F8	F4	F2	F1	CODE F( )
0	Read Group 1 Register	0	0	0	0	0	0
1	Read Group 2 Register	0	0	0	0	1	1
2	Read and Clear Group 1 Register	0	0	0	1	0	2
3	Read Complement of Group 1 Register	0	0	0	1	1	3
4	Non standard	0	0	1	0	0	4
5	Reserved	0	0	1	0	1	5
6	Non standard	0	0	1	1	0	6
7	Reserved	0	0	1	1	1	7
8	Test Look at Me	0	1	0	0	0	8
9	Clear Group 1 Register	0	1	0	0	1	9
10	Clear Look at Me	0	1	0	1	0	10
11	Clear Group 2 Register	0	1	0	1	1	11
12	Non standard	0	1	1	0	0	12
13	Reserved	0	1	1	0	1	13
14	Non standard	0	1	1	1	0	14
15	Reserved	0	1	1	1	1	15
16	Overwrite Group 1 Register	1	0	0	0	0	16
17	Overwrite Group 2 Register	1	0	0	0	1	17
18	Selective Set Group 1 Register	1	0	0	1	0	18
19	Selective Set Group 2 Register	1	0	0	1	1	19
20	Non standard	1	0	1	0	0	20
21	Selective Clear Group 1 Register	1	0	1	0	1	21
22	Non standard	1	0	1	1	0	22
23	Selective Clear Group 2 Register	1	0	1	1	1	23
24	Disable	1	1	0	0	0	24
25	Execute	1	1	0	0	1	25
26	Enable	1	1	0	1	0	26
27	Test Status	1	1	0	1	1	27
28	Non standard	1	1	1	0	0	28
29	Reserved	1	1	1	0	1	29
30	Non standard	1	1	1	1	0	30
31	Reserved	1	1	1	1	1	31

DATAWAY TIMING *



*Idealized

PIN ALLOCATION AT NORMAL STATION

(Stations 1-24)

Bus-line	Free Bus-line	P1	B	Busy	Bus-line
Bus-line	Free Bus-line	P2	F16	Function	Bus-line
Individual patch contact		P3	F8	Function	Bus-line
Individual patch contact		P4	F4	Function	Bus-line
Individual patch contact		P5	F2	Function	Bus-line
Bus-line	Command Accepted	X	F1	Function	Bus-line
Bus-line	Inhibit	I	A8	Sub-address	Bus-line
Bus-line	Clear	C	A4	Sub-address	Bus-line
Individual line	Station Number	N	A2	Sub-address	Bus-line
Individual line	Look-at-Me	L	A1	Sub-address	Bus-line
Bus-line	Strobe 1	S1	Z	Initialize	Bus-line
Bus-line	Strobe 2	S2	Q	Response	Bus-line
		W24	W23		
		W22	W21		
		W20	W19		
		W18	W17		
		W16	W15		
		W14	W13		
		W12	W11		
		W10	W9		
		W8	W7		
		W6	W5		
		W4	W3		
		W2	W1		
		R24	R23		
		R22	R21		
		R20	R19		
		R18	R17		
		R16	R15		
		R14	R13		
		R12	R11		
		R10	R9		
		R8	R7		
		R6	R5		
		R4	R3		
		R2	R1		
Power Bus-lines	−12V d.c.	−12	−24	−24V d.c.	Power Bus-lines
	+200V d.c.	+200	−6	−6V d.c.	
	117V a.c. Live	ACL	ACN	117V a.c. Neutral	
	Reserved	Y1	E	Clean Earth	
	+12V d.c.	+12	+24	+24V d.c.	
	Reserved	Y2	+6	+6V d.c.	
	OV (Power Return)	0	0	OV (Power Return)	

24 Write Bus Lines

W1 = least significant bit
W24 = most significant bit

24 Read Bus Lines

R1 = least significant bit
R24 = most significant bit

PIN ALLOCATION AT CONTROL STATION

(Station 25)

Individual patch contact		P1	B	Busy	Bus-line
Individual patch contact		P2	F16	Function	Bus-line
Individual patch contact		P3	F8	Function	Bus-line
Individual patch contact		P4	F4	Function	Bus-line
Individual patch contact		P5	F2	Function	Bus-line
Bus-line	Command Accepted	X	F1	Function	Bus-line
Bus-line	Inhibit	I	A8	Sub-address	Bus-line
Bus-line	Clear	C	A4	Sub-address	Bus-line
Individual patch contact		P6	A2	Sub-address	Bus-line
Individual patch contact		P7	A1	Sub-address	Bus-line
Bus-line	Strobe 1	S1	Z	Initialize	Bus-line
Bus-line	Strobe 2	S2	Q	Response	Bus-line
		L24	N24		
		L23	N23		
		L22	N22		
		L21	N21		
		L20	N20		
		L19	N19		
		L18	N18		
		L17	N17		
		L16	N16		
		L15	N15		
		L14	N14		
24 Individual Look-at-Me Lines		L13	N13	24 Individual Station Number Lines	
L1 from Station 1, etc.		L12	N12	N1 to Station 1, etc.	
		L11	N11		
		L10	N10		
		L9	N9		
		L8	N8		
		L7	N7		
		L6	N6		
		L5	N5		
		L4	N4		
		L3	N3		
		L2	N2		
		L1	N1		
Power Bus-lines	−12V dc.	−12	−24	−24V d.c.	Power Bus-lines
	+200V d.c.	+200	−6	−6V d.c.	
	117V a.c. Live	ACL	ACN	117V a.c. Neutral	
	Reserved	Y1	E	Clean Earth	
	+12V d.c.	+12	+24	+24V d.c.	
	Reserved	Y2	+6	+6V d.c.	
	OV (Power Return)	0	0	OV (Power Return)	

STANDARD DATAWAY USAGE

TITLE	DESIGNATION	CON-TACTS	USE AT A MODULE
Command			
Station Number	N	1	Selects the module (Individual line from control station)
Sub-Address	A1, 2, 4, 8	4	Selects a section of the module.
Function	F1, 2, 4, 8, 16	5	Defines the function to be performed in the module.
Timing			
Strobe 1	S1	1	Controls first phase of operation (Dataway signals must not change)
Strobe 2	S2	1	Controls second phase (Dataway signals may change).
Data			
Write	W1 – W24	24	Bring information to the module.
Read	R1 – R24	24	Take information from the module.
Status			
Look at-Me	L	1	Indicates request for service (Individual line to control station)
Busy	B	1	Indicates that a Dataway operation is in progress.
Response	Q	1	Indicates status of feature selected by command.
Command Accepted	X	1	Indicates that module is able to perform action required by the command.
Common Controls			*Operate on all stations connected to them, no command required.*
Initialize	Z	1	Sets module to a defined state. (Accompanied by S2 and B).
Inhibit	I	1	Disables features for duration of signal.
Clear	C	1	Clears registers. (Accompanied by S2 and B)
Non-Standard Connections			
Free bus-lines	P1, P2	2	For unspecified uses.
Patch contacts	P3 P5	3	For unspecified interconnections. No Dataway Lines.
Mandatory Power Lines			*The crate is wired for mandatory and additional lines.*
+24V d.c	+24	1	
+6V d.c.	+6	1	
−6V d.c.	−6	1	
−24V d.c.	−24	1	
OV	0	2	Power return.
Additional Power Lines			*Lines are reserved for the following power supplies.*
+200V d.c.	+200	1	Low current for indicators etc
+12V d.c.	+12	1	
−12V d.c.	−12	1	
117V a.c. (Live)	ACL	1	
117V a.c. (Neutral)	ACN	1	
Clean Earth	E	1	Reference for circiuts requiring clean earth
Reserved	Y1, Y2	2	Reserved for future allocation
TOTAL		86	

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technical information

BASIC CAMAC DATAWAY OPERATING INFORMATION

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INTRODUCTION

CAMAC is an international standard of modularized electronics as defined by the ESONE Committee of the JNRC, Ispra. Its function is to provide a scheme to allow a wide range of modular instruments to be interfaced to a standardized multi-receptacle which, in turn, may be interfaced to a computer. In this way, additions to a data transfer and control system may be made by plugging-in additional modules and making suitable software changes. Thus, CAMAC allows information to be transfered into and out of the instrument modules.

CAMAC modules may be plugged into a CAMAC Crate which has 25 Stations, numbered 1 through 25. Station 25, the rightmost station, is reserved for a Crate Controller, whereas Stations 1 - 24 are Normal Stations used for CAMAC Modules. Usually, Station 24 is also used by the controller in that most controllers are double width (#2 CAMAC). The purpose of the controller is to issue CAMAC Commands to the modules and transfer information between a computer (or other digital device) and the CAMAC modules.

Data transfer, control functions, and module powering is affected via the Dataway. This is a series of bus and individual lines across the back of the crate. The dataway lines include digital data transfer lines, strobe signal lines, and addressing lines and control lines. See Page 18C for a pin allocation chart.

In a typical dataway operation, the crate controller issues a CAMAC Command which includes specifying a station number (N), a subaddress (A), and function code (F) (see Page 17C). In response, the subaddress of the module will generate valid command accepted (X response) and act on the command. If this command requires data transfer, the read (R) or write (W) lines will be used. Note that the terms Read and Write apply to the controller, not the module. For example, under a read command, the controller reads data contained within a module.

USE OF THE DATAWAY LINES

Communication with plug-in units takes place through the Dataway. This passive multi-wire highway is incorporated in the crate and links the 86-pin sockets to all stations. The bus-lines link corresponding pins at all normal stations and, in some cases, the control station. Individual lines link one pin at a normal station to one pin at the control station. The patch pins have no specified Dataway wiring but can be connected to individual points to which patch leads may be attached.

During a Dataway operation the controller generates a command consisting of signals on individual Station Number lines to specify one or more modules, signals on the Subaddress bus-lines to specify a sub-section of the module or modules, and signals on the Function bus-lines to specify the operation to be performed. The command signals are accompanied by a signal on the Busy bus-line, which is available at all stations to indicate that a Dataway operation is in progress.

When a module recognizes a Read command, calling for a data transfer to the controller, it establishes data signals on the Read bus-lines. When a controller recognizes a Write command calling for a data transfer to a module, it establishes data signals on the Write bus lines. In addition, regardless of whether there is transfer on the R or W lines, the module may transmit one bit of status information on the Response bus-line.

Two timing signals, Strobes S1 and S2, are then generated in sequence on separate bus-lines. The strobes are used to transfer data from the Dataway into modules (on Write commands) and into the controller (on Read commands). They may also initiate other actions within the controller and modules.

Whenever there is no Dataway operation in progress (indicated by the absence of the Busy signal) any module may generate a signal on its individual Look-at-Me line to indicate that is requires attention. Three common controll signals are available at all stations, without requiring addressing by a command, in order to Initialize all units (typically after switch-on), to Clear data registers, and to Inhibit features such as data-taking.

DEFINITION OF COMMANDS

A command consists of signals on the Dataway lines which specify at least one module (by individual station number lines), a sub-section of the module or modules (by the four sub-address bus-lines), and the function to be performed (by the five function bus-lines). The command signals are maintained for the full duration of the operation on the Dataway. They are accompanied by a signal on the Busy bus-line which indicates to all units that a Dataway operation is in progress.

Station Number (N)

Each normal station is addressed by a signal on an individual station number line (N) which comes from a separate pin at the control station. The stations are numbered in decimal code from the left-hand end as viewed from the front, beginning with Station 1.

Sub-Address (A8, A4, A2, A1)

Different sections of a module are addressed by signals on the four A bus-lines. These signals are decoded in the module to select one of up to sixteen sub-addresses, numbered in decimal from 0 to 15.

Function (F16, F8, F4, F2, F1)

The function to be performed at the specified sub-address in the selected module or modules is defined by the signals on the five F bus-lines. These signals are decoded in the module to select one of up to 32 functions, numbered in decimal from 0 to 31. The definitions of the 32 function codes are summarized in the Dataway Command Operations section.

Strobe Signals (S1 and S2)

Two strobe signals S1 and S2 are generated in sequence on separate bus-lines. These signals are used to transfer information between plug-in units via the Dataway or to initiate operations within units. In either case the specific action is determined by the command present on the Dataway. Both strobes are generated during each Dataway command operation, and all plug-in units which accept information from the Dataway do so in response to these strobes. The first strobe S1 is used for actions which do not change the state of signals on the Dataway lines. All units which accept data from the Dataway in a Read operation, or in a Write operation do so in response to S1. The second strobe S2 is used to initiate any actions which may change the state of Dataway signals, for example, clearing a register whose output is connected to the Dataway.

DATA

A common parallel highway is used for all transfers. All information carried by the parallel highway is conveniently described as data, although it may be information concerned with status or control features in modules. Up to 24 bits may be transferred in parallel between the controller and the selected module. Independent lines (Read and Write) are provided for the two directions of transfer.

The Write Lines (W1-W24)

The controller or other common data source generates data signals on the W bus-lines at the beginning of any 'Write' operation. The W signals reach a steady state before S1, and are maintained until the end of the operation, unless modified by S2.

The Read Lines (R1-R24)

Data signals are set up on the R bus-lines by the module as soon as a "Read" command is recognized. The R signals reach a steady state before S1, and are maintained for the full duration of the Dataway operation, unless the state of the data source is changed by S2. The controller or other common data receiver strobes the data from the R bus-lines at the time of the Strobe S1.

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